PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

Transmission Electron Microscopy of Micro- and Nanostructures in Semiconductors

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Transmission electron microscopy of micro- and nanostructures in semiconductors

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Semiconducting materials science and technology are extremely active areas of research because they underpin advanced electronic device fabrication. Electron microscopy studies of the materials play a vital role in the work, since they provide uniquely detailed structural and chemical information on all important length scales. The present article reviews applications of, primarily, transmission electron microscopy in critical areas ranging from epitaxial growth through to final device analysis. The examples provided demonstrate the comprehensive assessment of materials structure and composition which can be achieved.

1. Introduction

Advanced semiconductor devices exploit complex structures and designs which require the use of extended sophisticated processing sequences for fabrication. The emphasis in such procedures is upon the control of the micro- and nanostructure of semiconductors and related materials to ensure that the finished devices exhibit the expected electrical and/or optical characteristics.

In order to control the structure of semiconducting materials it is necessary that their behaviour during processing is fully understood. In this regard, the electron microscope is unsurpassed in its ability to deliver imaging, diffraction and related information on materials structure and composition for all scales down to that of the atom. The present paper describes applications of, principally, the transmission electron microscope (TEM) to many of the areas of importance across the spectrum of semiconductor studies. The work reviewed has great importance for both fundamental science and advanced device technology.

2. Layer growth phenomena

The growth of epitaxial layers is an important element of semiconductor technology for a number of reasons. Homoepitaxial layers on bulk substrates are often required when surface or buried strata with specific doping levels are needed for particular device structures. Furthermore, the heteroepitaxial growth of different materials, one upon the other, is in general employed to exploit varied structural, optical or electronic properties in combination, often for advanced device fabrication. In this latter case, when the level of mismatch between the different materials is low, one of the main characteristics of interest is layer compositional uniformity and the sharpness of

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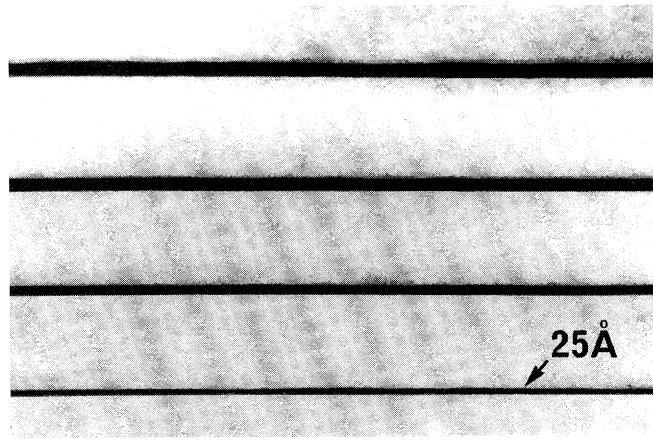

Figure 1. TEM cross-sectional image, bright-field, 200 reflection, of InGaAs quantum wells (dark) in InP. (After Cullis 1990.)

heterointerfaces. A typical structure grown by metal-organic chemical vapour deposition (MOCVD) and having InGaAs quantum wells within an InP matrix is shown in the TEM image of figure 1 (Cullis 1990), obtained using a chemically sensitive 200 Bragg reflection. In order to verify the compositional variations within such a structure, a standard analysis typically would employ secondary ion mass spectrometry, which can reveal composition variations with a depth resolution of *ca.* 2 nm. However, if there are small-scale lateral non-uniformities, the accuracy of such an analysis will be degraded.

When excellent depth and lateral resolutions are required simultaneously, it is necessary to employ electron probe analytical techniques. One important approach exploits the very small (less than *ca.* 1 nm) electron probe produced by a microscope with a field emission electron gun. The spot is then scanned in steps across the appropriate region of a thin cross-sectional sample and the emitted X-rays are analysed to obtain the local specimen compositions. This is demonstrated (McGibbon *et al.* 1989) in figure 2, which shows an analysis of interface sharpness in a structure of the type shown in figure 1 but grown under non-optimum reactor conditions. While the InP–InGaAs interface is sharp, the InGaAs–InP interface displays principally As (but also Ga) carry-over into the adjacent InP barrier. The spatial resolution achieved in this analysis approaches 1 nm and gives important information upon the manner in which gas switching must be optimized during MOCVD layer growth.

Atomic-scale spatial resolution of composition may be obtained by the analysis of high-resolution TEM images. This can be achieved in a number of ways, one employing multi-dimensional vector analysis of image contrast (Ourmazd *et al.* 1989). However, there is a more direct approach (Thoma & Cerva 1991; Walther & Gerthsen 1993) using Fourier transformation of a geometrically regularized image and then calculation of a chemically sensitive Bragg reflection amplitude at the location of each visible atomic column. An example of the results of this procedure is shown in figure 3. Figure 3*a* shows a conventional [100] cross-sectional bright-field image of GaAs quantum wells (dark) grown by MBE in AlAs (bright). At this level of resolution, all well interfaces appear similarly sharp. However, upon application of the above analytical procedure to a high-resolution image obtained from the upper narrow quantum well, atomic-scale compositional information is obtained (Walther &

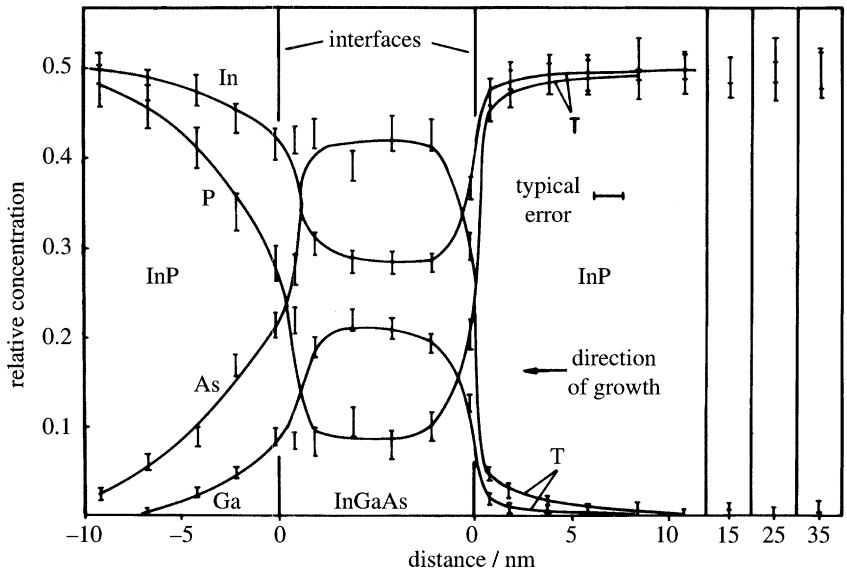

Figure 2. Variation of composition, expressed in terms of atomic fractions, across a 10 nm MOCVD InGaAs quantum well in InP. Note asymmetry of elemental distributions. (After McGibbon *et al.* 1989.)

Gerthsen 1993) as illustrated in figure 3*b*. The layer growth direction runs from bottom to top of the micrograph and it is immediately clear that, while the GaAs–AlAs interface has a width of about two monolayers, the AlAs–GaAs interface has a significantly greater width of about three monolayers. Asymmetrical interface broadening of this type may be associated with the relatively low mobility of Al on the crystal growth surface (Madhukar 1988) and directly affects the opto-electronic properties of the quantum well structures.

When the lattice mismatch between the heteroepitaxial materials is significant, this leads to the occurrence of large stresses within a deposited layer. In such circumstances, as the thickness of the layer increases, the original work of Frank & van der Merwe (1949) and Matthews (1975) demonstrated that a critical thickness will be reached at which stress-relieving dislocations are introduced into the system, at first by the bending over of preexisting threading dislocations into the interface. At later stages of stress relief there is evidence that new misfit dislocation sources operate including, for example in the SiGe–Si system, the so-called 'diamond defect' (Humphreys *et al.* 1991) and recently proposed interfacial stress centres arising from regions of composition fluctuation (Perovic & Houghton 1995). Much of the extensive work (see, for example, Fitzgerald 1991) which has been carried out to determine the nature of heteroepitaxial stress-relief processes has relied upon TEM observations to provide the high spatial resolution and local strain sensitivity needed. Indeed, in systems of large misfit, at the level of lattice resolution it is possible to image interfacial defects only a few lattice spacings apart. This is illustrated in figure 4, where a high resolution TEM image shows the heteroepitaxial interface for CdTe grown by MOCVD on GaAs (Cullis 1990). Due to the very large lattice misfit (*ca.* 14.7%), a very closely spaced network of interfacial dislocations has been produced. The image confirms that the dislocations are primarily of Lomer edge-type (with some 60°-type) and have a mean spacing of *ca.* 3 nm, which is in good accord with the separation required to relieve the lattice misfit.

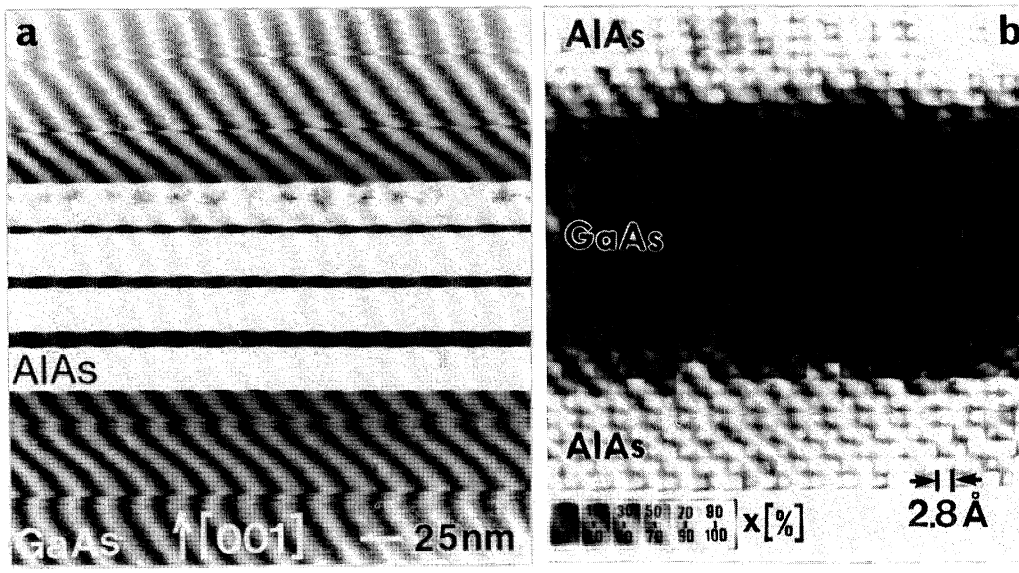

Figure 3. TEM cross-sectional images: (*a*) 200 dark-field, of GaAs quantum wells (dark) in AlAs; (*b*) processed HREM image of GaAs–AlAs quantum well showing composition variations. (After Walther & Gerthsen 1993.)

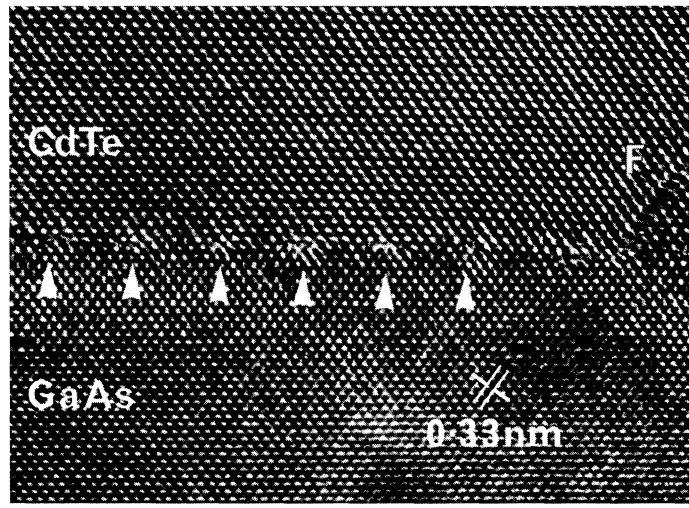

Figure 4. HREM cross-sectional image along [110] direction of misfit dislocations (arrowed) at CdTe–GaAs heterointerface. Stacking fault (F) also shown. (After Cullis *et al.* 1985.)

Before plastic stress-relief of the type just described occurs in an heteroepitaxial layer with large misfit, elastic stress-relief may take place by rippling of the growth surface The occurrence of this phenomenon was theoretically predicted (Srolovitz 1989) and later observed (Cullis *et al.* 1992) in the SiGe–Si system. Figure 5 presents plan-view TEM images of ripple arrays which form on a compressively strained $Si_{0.8}Ge_{0.2}$ layer grown on Si by low pressure CVD at 750 °C. The quasi-kinematical image in figure 5*a* shows the general nature of the ripples using mass-thickness contrast. However, the other sections of figure 5 show the pronounced dark–bright con-

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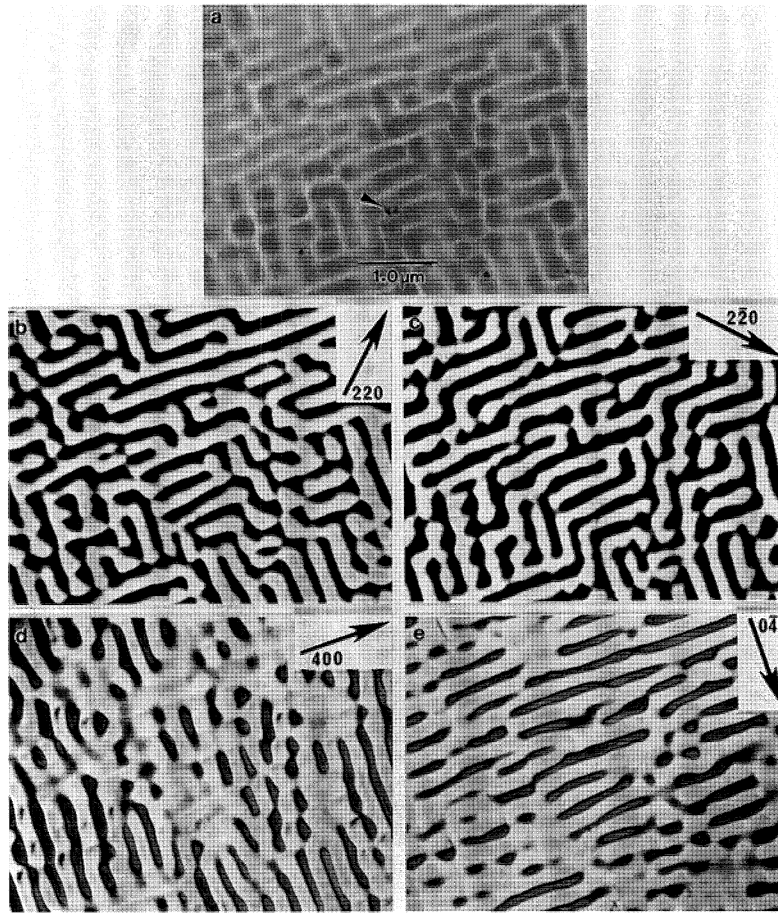

Figure 5. TEM plan-view images of the same area of ripples on a growth surface of SiGe–Si. Note contrast variation with change in operating Bragg reflection. (After Cullis *et al.* 1992.)

trast which is given by imaging with strongly excited Bragg reflections. Analysis of this contrast (Cullis *et al.* 1992) shows that layer relaxation takes place by expansion of the vertical lattice planes within the ripple crests: this is accompanied by a very localized additional compression of the lattice beneath the ripple troughs.

The type of morphological distortion of a heteroepitaxial layer just described has significance for a number of aspects of layer behaviour. It is possible that, due to stress-driven flows of surface atoms during growth, unstable cusps may form in the surface (Jesson *et al.* 1993). An example of this is presented in figure 6, where the surface of a SiGe layer is depicted as a function of time by thin Ge marker layers (light) deposited during the growth. The development of the cusp can be modelled by considering the kinetics of surface atom diffusion, as illustrated in the lower half of the figure. Furthermore, in a manner originally predicted for general surface depressions (Freund *et al.* 1989), additional compressive stress at the above-described ripple troughs or cusps can give rise to misfit dislocation nucleation. This is clearly illustrated in the high resolution TEM image of figure 7, which demonstrates (Cullis *et al.* 1995) the formation of a Frank partial dislocation segment, with associated stacking fault, beneath a ripple trough and close to the interfacial plane for an undulating

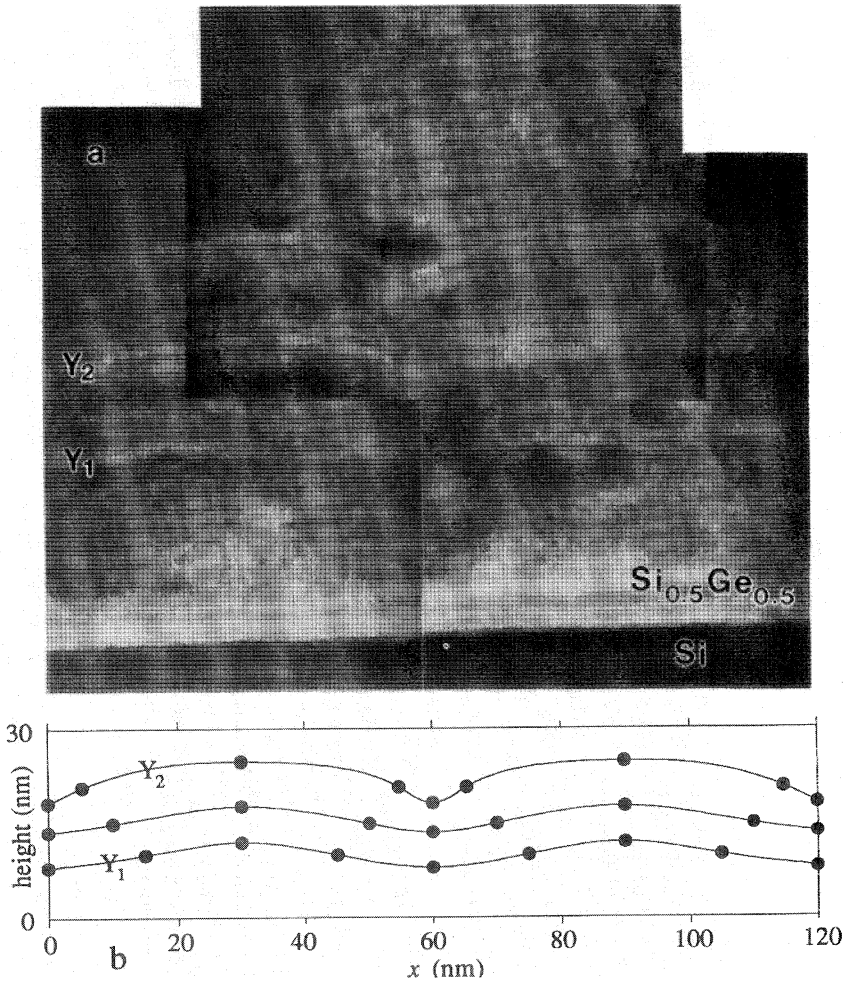

Figure 6. (*a*) STEM cross-sectional image of unstable cusp formation in SiGe–Si growth surface. (*b*) Theoretical simulation of surface profile is shown in lower part of figure. (After Jesson *et al.* 1993.)

InGaAs layer grown on GaAs (misfit 1.8%). It appears that such misfit dislocations form by point defect (vacancy) aggregation in this region of increased compressive stress. They may then transform into commonly seen Lomer dislocations (or fault pairs as shown) by suitable Shockley partial emission. For sessile Lomer dislocation formation, the following reaction would apply:

$$(a/3)[\bar{1}1\bar{1}] \rightarrow (a/6)[\bar{2}\bar{1}1] + (a/2)[01\bar{1}].$$

Thus, it is evident that the surface morphology of a heteroepitaxial layer can critically control the manner in which defects are introduced during layer growth.

3. Layer processing phenomena

Modern device fabrication requires semiconductor processing steps which are extremely carefully devised and controlled. The final device structures are very tightly

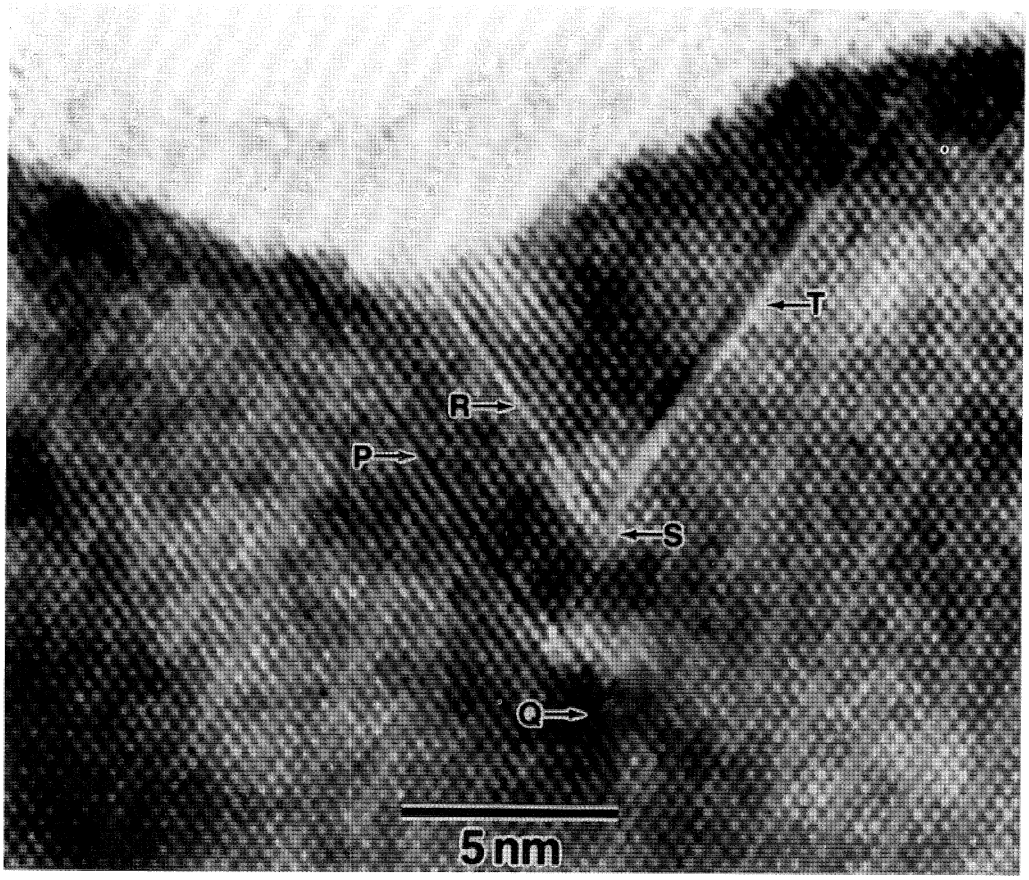

Figure 7. Cross-sectional high resolution TEM image, [011] surface normal, showing misfit defects nucleated at surface ripple trough: stacking fault (P) bounded by Frank partial dislocation (Q—note terminating lattice fringe parallel to fault plane) and stacking fault (R) bounded by stair-rod dislocation (S) leading to secondary fault (T). (After Cullis *et al.* 1995.)

packed and complex, so that only the TEM is capable of revealing some of the finest features. The situation is illustrated in figure 8, which shows (Cunningham 1995) two cells of a 256 Mb dynamic random access memory (DRAM) integrated circuit (IC). The poly-Si-filled trench capacitors required for charge storage are clearly visible, as are the wordline (WL) and bitline conductors near the top of the image. Indeed, TEM techniques have been important in the development of silicide technology for interconnect and contact applications (see, for example, Murarka 1983). Cross-sectional views of the type shown in figure 8 allow device engineers to verify that the intended structural layout has been achieved after a very large number of processing steps. In addition, internal strains which build up during the fabrication of such multilevel structures can be directly measured by analysis of TEM image contrast and the use of associated diffraction techniques (Armigliato *et al.* 1993). One of the most critical features of a DRAM IC is the field effect transistor (FET) gate oxide which must be of high quality with a thickness which is accurately tailored, often at the 5–10 nm level. Such an oxide beneath a poly-Si gate electrode is shown in figure 9, where a small variation in oxide thickness is apparent. In order to

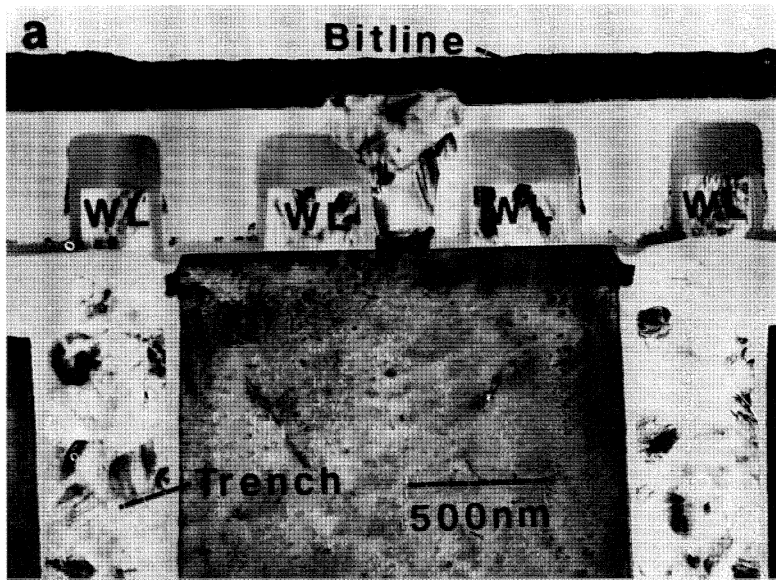

Figure 8. TEM cross-sectional image of 256 Mb DRAM device structures showing layout of two cells. (After Cunningham *et al.* 1995.)

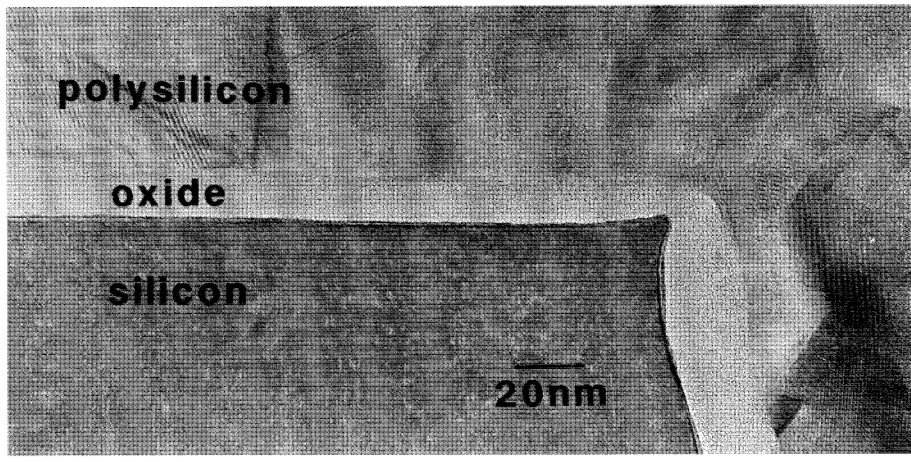

Figure 9. TEM cross-sectional image of an FET thin gate oxide, showing thickness variations. (After Cunningham *et al.* 1995.)

optimize electrical characteristics, greater uniformity would be required in the final device structure.

The integrity of gate oxide layers is of the greatest importance in controlling Si FET performance and primary factors which can adversely influence it are the presence of transition element impurities, buried near-surface oxide precipitates and surface micro-roughness (Ohmi *et al.* 1992). The unwanted impurities most commonly encountered are the fast-diffusing transition elements Cu, Fe and Ni and their influence varies, depending upon the concentration at which they are present. They generally introduce deep electronic levels into the Si but, at relatively high concentrations, they can precipitate within Si device regions as silicides. An example of such

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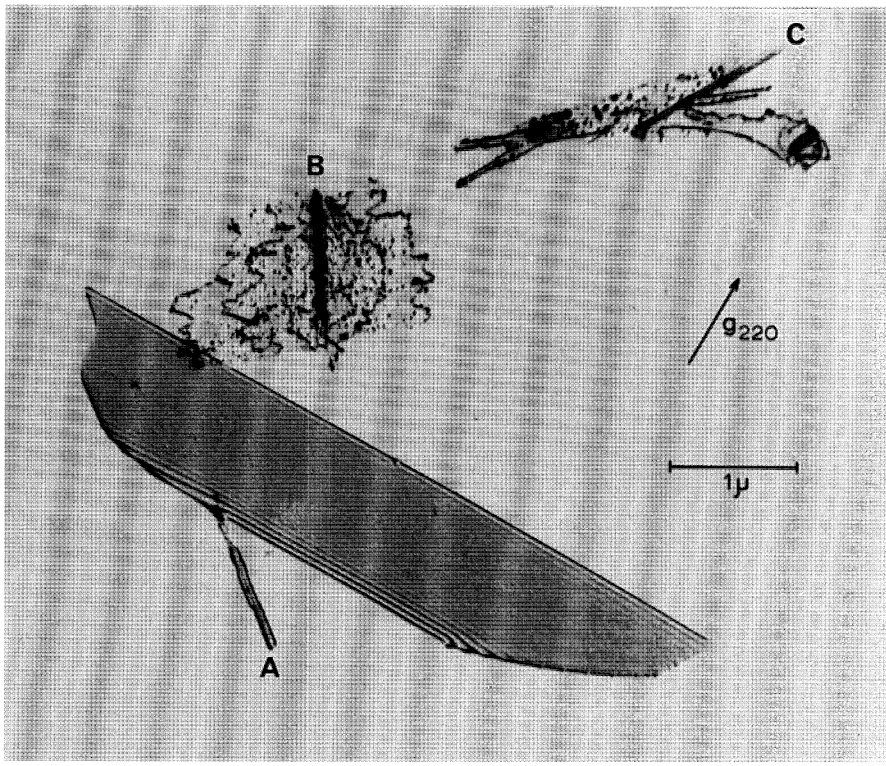

Figure 10. TEM image showing inclined rod-like $FeSi_2$ precipitates A, B and C in Si, the latter two also exhibiting subsidiary copper silicide precipitation. The boat-shaped feature is an oxidation-induced stacking fault. (After Cullis & Katz 1974.)

precipitation is shown in figure 10, where inclined ζ_α–$FeSi_2$ rods have formed during bipolar transistor processing (Cullis & Katz 1974). These rods have high electrical conductivity and, therefore, cause local short-circuits as well as introducing carrier generation–recombination zones. In addition, some of the rods are seen to have given rise to wing-like dislocation structures which have formed by climb under the influence of point defects produced by subsidiary Cu precipitation as silicide particles around $FeSi_2$ rods. An oxidation-induced stacking fault is also visible in the imaged area.

Clearly, the concentration of transition elements in device regions must be reduced to the minimum possible level and this is generally achieved by use of one or more gettering procedures during material processing (Gilles & Ewe 1994; Sano *et al.* 1994). An important approach involves the use of oxygen in solution within the Si of a Czochralski wafer (internal gettering). Upon receiving the first high temperature heat treatment in the processing sequence, this oxygen precipitates as microscopic amorphous SiO_2 particles (identified by nanoprobe electron energy loss analysis (Carpenter *et al.* 1989)) within the bulk of the wafer, while leaving precipitate-free denuded zones near each surface. During subsequent processing, because the particles strain the Si matrix, they punch out arrays of dislocation loops and these then act as nucleation sites for transition element silicides. This is illustrated in figure 11, which shows $NiSi_2$ precipitates formed in the manner described (Bhatti *et al.* 1991). The gettering of transition elements so achieved removes them from device active re-

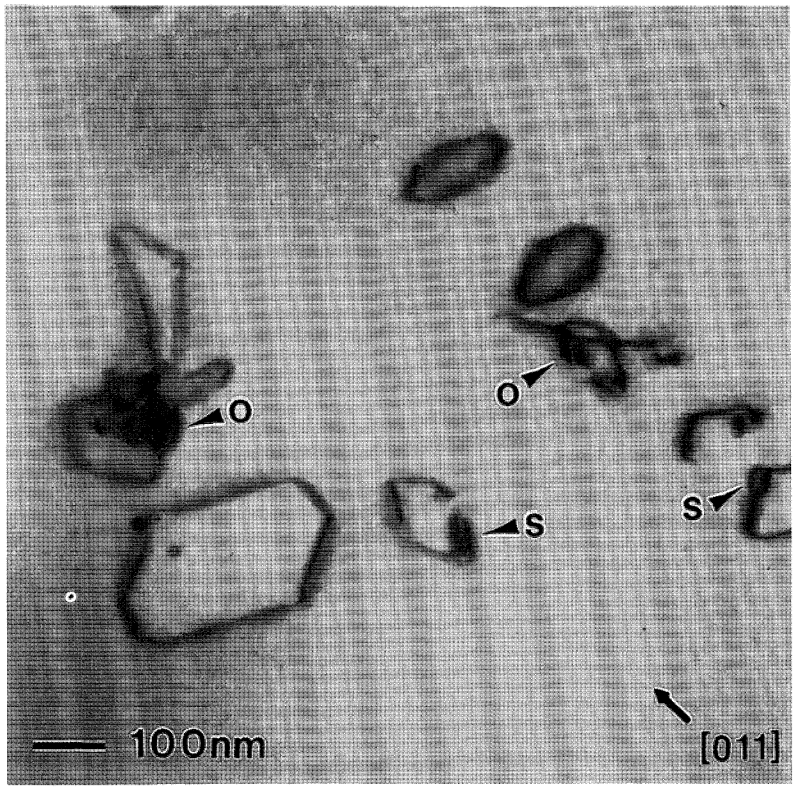

Figure 11. TEM image of bulk Si, showing oxide precipitate particles (O), with array of punched-out dislocation loops which getter impurity $NiSi_2$ precipitates (S). (After Bhatti *et al.* 1992.)

gions. However, it is also critical that there should be few if any SiO_2 particles in the near-surface denuded zones, since these would very adversely affect FET gate oxides. Indeed, it has been shown that this can be achieved highly effectively by high temperature annealing in a hydrogen atmosphere (Kubota *et al.* 1994). Other (external) gettering techniques which may be employed to remove transition metal impurities from device regions generally involve treatments of the back of the wafer. These include phosphorus diffusion gettering which appears to remove transition elements by local solubility enhancement (Meek *et al.* 1975) together with precipitation, and backside damage and poly-Si deposition gettering which trap such impurities principally by precipitation at defect sites. Inert gas ion implantation in Si, followed by annealing, can yield densely disordered layers appropriate for gettering purposes (see, for example, Cullis *et al.* 1978): these layers contain cavities and it is possible that gettering of transition elements by the cavities (Follstaedt & Myers 1995) is more effective than gettering by precipitate phase formation at other layer defect structures.

Precipitate phases of many different types form in a wide range of semiconducting materials and TEM studies are vital in their identification. Another important example is that of precipitates which are produced in single-crystal GaAs ingots during their growth. Such particles are generally 10–100 nm in diameter and are often found attached to dislocations within the crystal (see figure 12). The precipi-

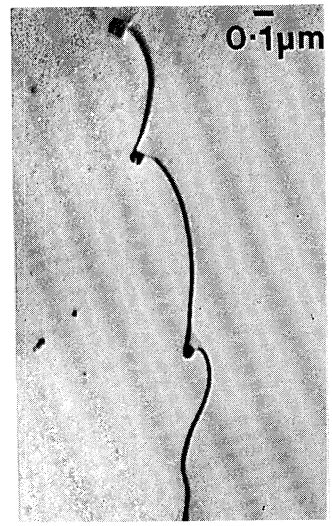

Figure 12. TEM image of elemental As precipitates attached to dislocation in bulk GaAs. (After Cullis *et al.* 1980.)

tates have been identified as crystalline elemental As by detailed diffraction analysis (Cullis *et al.* 1980), with implications concerning the great mobility of As interstitials in the III–V lattice. Furthermore, the presence of As precipitates in GaAs device material can have a very deleterious effect upon electronic devices (particularly FETs) subsequently fabricated (Oda *et al.* 1992).

One of the most widely exploited processing techniques is that of ion implantation (already mentioned above), which is almost universally used to introduce dopant species into device active areas. However, the large amount of lattice damage produced as the injected high energy dopant ions pass into the semiconductor must be restructured by annealing (Seidel 1983*a*) in order to obtain satisfactory dopant electrical activity. The effectiveness with which this can be achieved depends substantially upon the nature of the initial implant. High doses of very light ions, such as B^+, tend to yield initial buried damage bands (figure 13*a*) which give rise to unwanted residual dislocations after annealing (figure 13*b*). If the initial damage level is raised to that of full amorphization, either by preamorphization with another ion species (for example, Si^+) or by use of BF_2^+ implantation, much higher quality regrowth can be achieved (Seidel 1983*b*). In the same way, damage introduced by relatively heavy ions, such as As^+, rapidly saturates to the amorphous level and can yield excellent regrowth upon annealing (figures 13*c*, *d*). Complications can arise if ions are implanted through a thin surface layer of another material. For example, implantation through thin oxide layers can lead to significant recoil implantation of oxygen, which then degrades the quality of the subsequent annealed structure due to additional intractable defect formation (Moline & Cullis 1975). Such recoil implantation will be an important phenomenon at imperfectly sharp (graded) device window edges defined by patterned oxide and/or photoresist. This is expected to be especially significant where high implant doses are employed as in the case of, for example, the formation of patterned Sb-doped subcollectors employed in ULSI BICMOS technology (Bhattacharyya *et al.* 1994).

In many cases, such as for Si FET gates, relatively low implanted ion doses are

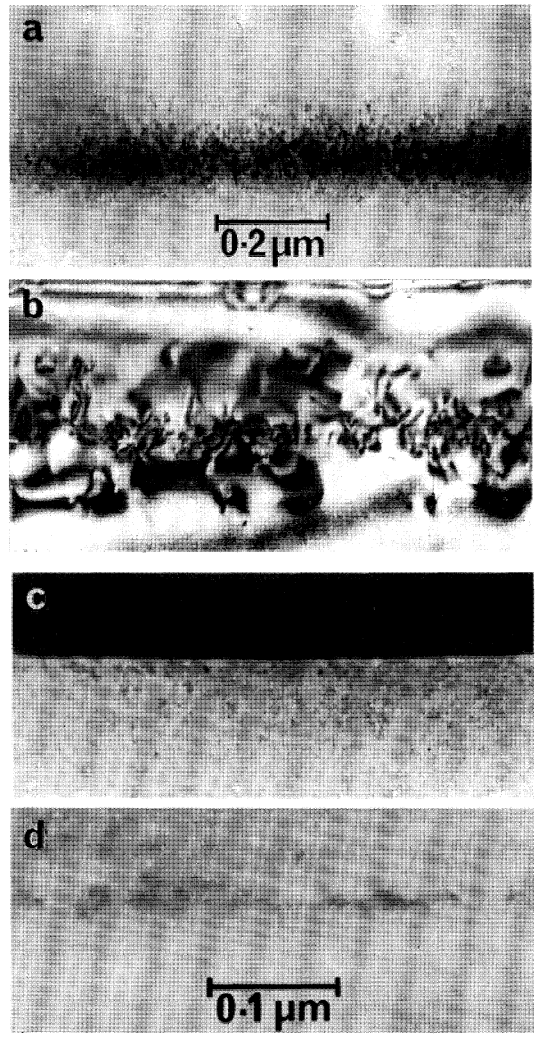

Figure 13. TEM cross-sectional images of as-implanted and annealed layers, respectively, for (*a*) and (*b*) B^+ ion implantation and (*c*) and (*d*) As^+ ion implantation. (After McMahon *et al.* 1980.)

required. In such circumstances, although few extended defects remain after final anneals, transient enhanced diffusion of the implanted dopant can take place. This is most undesirable since it alters the dopant distribution in an uncontrolled manner. While the phenomenon has been believed for some time to be due to the effects of interstitial Si atoms, recent TEM work (Eaglesham 1995) has quantified the behaviour and shown that the interstitials can transiently form [311]-aligned linear defects. These rapidly dissociate during later stages of the anneal releasing interstitials which cause the enhanced dopant diffusion. However, some of the [311] defects transform into perfect dislocation loops, as shown in figure 14, to yield the low loop-defect density often seen after such implants. This work has also suggested a strategy for trapping many of the implantation-induced Si interstitials and, therefore, suppressing the unwanted dopant diffusion.

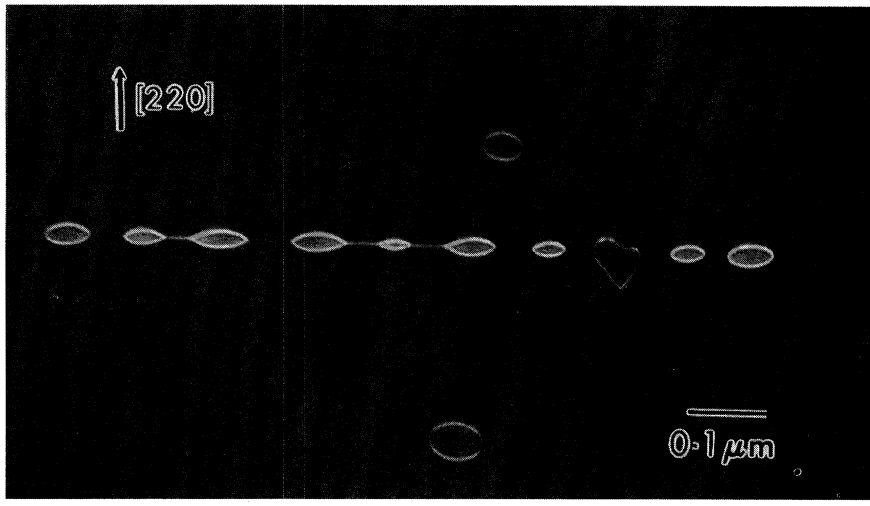

Figure 14. TEM image of dissociating ⟨311⟩ implantation defect giving dislocation loops. (After Eaglesham *et al.* 1995.)

Although, as noted above, recoil implantation of oxygen can give undesirable lattice damage during Si processing, the deliberate implantation of oxygen at extremely high doses is employed to form single crystal Si layers on buried insulating oxide (Hemment 1986), which can be used to provide enhanced device isolation. The implantation is carried out at high substrate temperature to yield partial *in situ* recrystallization. The wafer is subsequently reannealed at a temperature approaching the melting point in order to optimize the resulting structure and this is illustrated in the TEM images of figure 15. It is clear that for the highest temperature anneal shown, the structure of the surface Si layer is relatively good, although the Si–oxide interface quality requires further improvement and Si inclusions are present within the base of the oxide layer. The structure can be further refined by even higher temperature annealing, but it is difficult to remove all the Si inclusions from the oxide and some defects remain in the uppermost Si layer (Meda *et al.* 1994; Lee *et al.* 1994). The oxide inclusions have a significant effect upon electrical properties, reducing the effective thickness of the insulator and lowering its breakdown voltage. Alternative forms of Si-on-insulator are available (for example, material formed by direct wafer bonding) so that structural optimization can confidently be expected to progress further.

Conventional light-emitting devices are produced using compound semiconductors with direct bandgaps of magnitudes appropriate for the emission wavelengths required. Nevertheless, one key challenge which remains in Si-based electronics is to produce efficient light-emitting devices for integrated optical applications in this elemental material. However, only comparatively recently has this become a possibility. The observation (Canham 1990) that highly porous Si formed by anodization of crystalline wafers can emit photoluminescent radiation with very high efficiency has excited a large amount of interest. In order to understand the physical processes underlying the photoluminescence emission, it has been necessary to carry out careful TEM work upon the material (Cullis & Canham 1991). Indeed, as demonstrated in the image of figure 16*a* for an optimized supercritically dried layer (Canham *et al.* 1994), the material, of greater than 90% porosity, consists of undulating single crystal

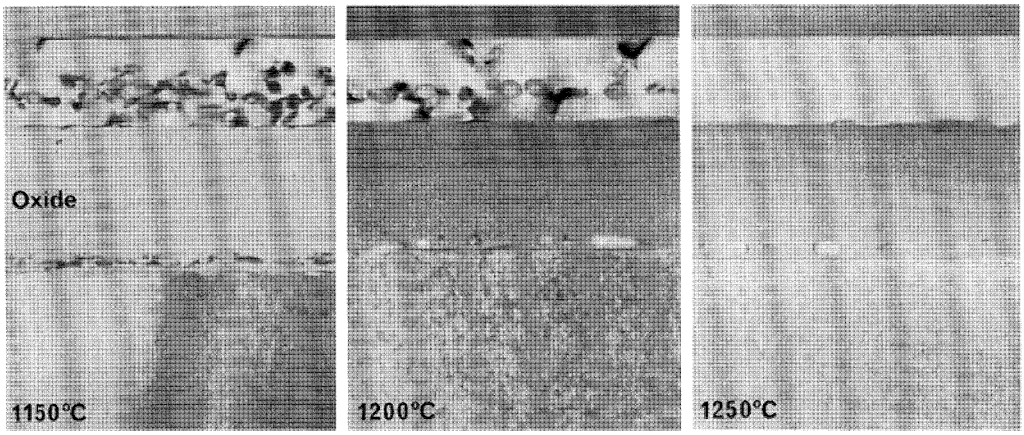

Figure 15. TEM cross-sectional images of SIMOX layers after post-implantation anneals at the indicated temperatures. (After Augustus 1995, personal communication.)

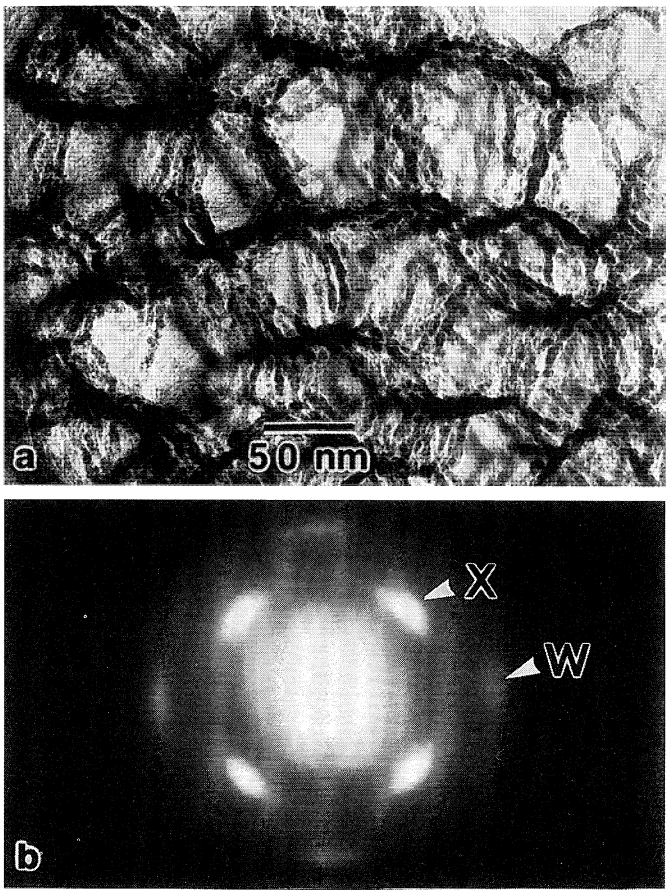

Figure 16. TEM study of nanostructures in supercritically dried porous Si: (*a*) TEM image showing undulating interconnected rods; (*b*) single crystal electron diffraction pattern showing 220 (X) and 400 (W) reflections. (After Canham *et al.* 1994.)

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

rods which are interconnected to give a coral-like open skeleton. Diffraction patterns (figure 16*b*) indicate that this skeleton is a single crystal, although there is a small dispersion of crystal orientations, revealed by slight arcing of the Bragg reflections, due to local flexing of the slender structural units. Photo-excited carriers are trapped within the rods (or quantum wires) which, due to their small dimensions, exhibit an increased bandgap (Read *et al.* 1992; Delerue *et al.* 1993). Subsequent recombination of these quantum-confined carriers leads to the emission of visible radiation often in the red region of the spectrum, but sometimes extending into the green. A major goal is to produce efficient electroluminescent devices and good progress has been made in this area (Loni *et al.* 1995). Furthermore, another approach for light emitting device fabrication involves the incorporation of Er into Si in the presence of oxygen (Benton *et al.* 1991; Eaglesham *et al.* 1991): this is also showing a great deal of promise, so that all-Si optoelectronic circuits may become a reality in the foreseeable future.

4. Conclusions

Semiconductors are produced as single crystals with purity and perfection greater than those of any other material. This then gives a unique opportunity to study a wide range of fundamental solid state phenomena in systems close to ideality. Electron microscopy work provides very detailed analytical information with relevance extending to many other materials systems. Furthermore, semiconductor device processing technology is becoming rapidly more sophisticated and increasingly dependent upon the control of extremely small-scale structures. As is clear from the examples presented above, electron microscopy, and in particular the TEM, is yielding vital insight into the finest details of materials behaviour and is underpinning advances vital to the device industry. These trends appear set to continue and, therefore, to demand ever greater progress in the structural and chemical analysis of semiconducting materials.

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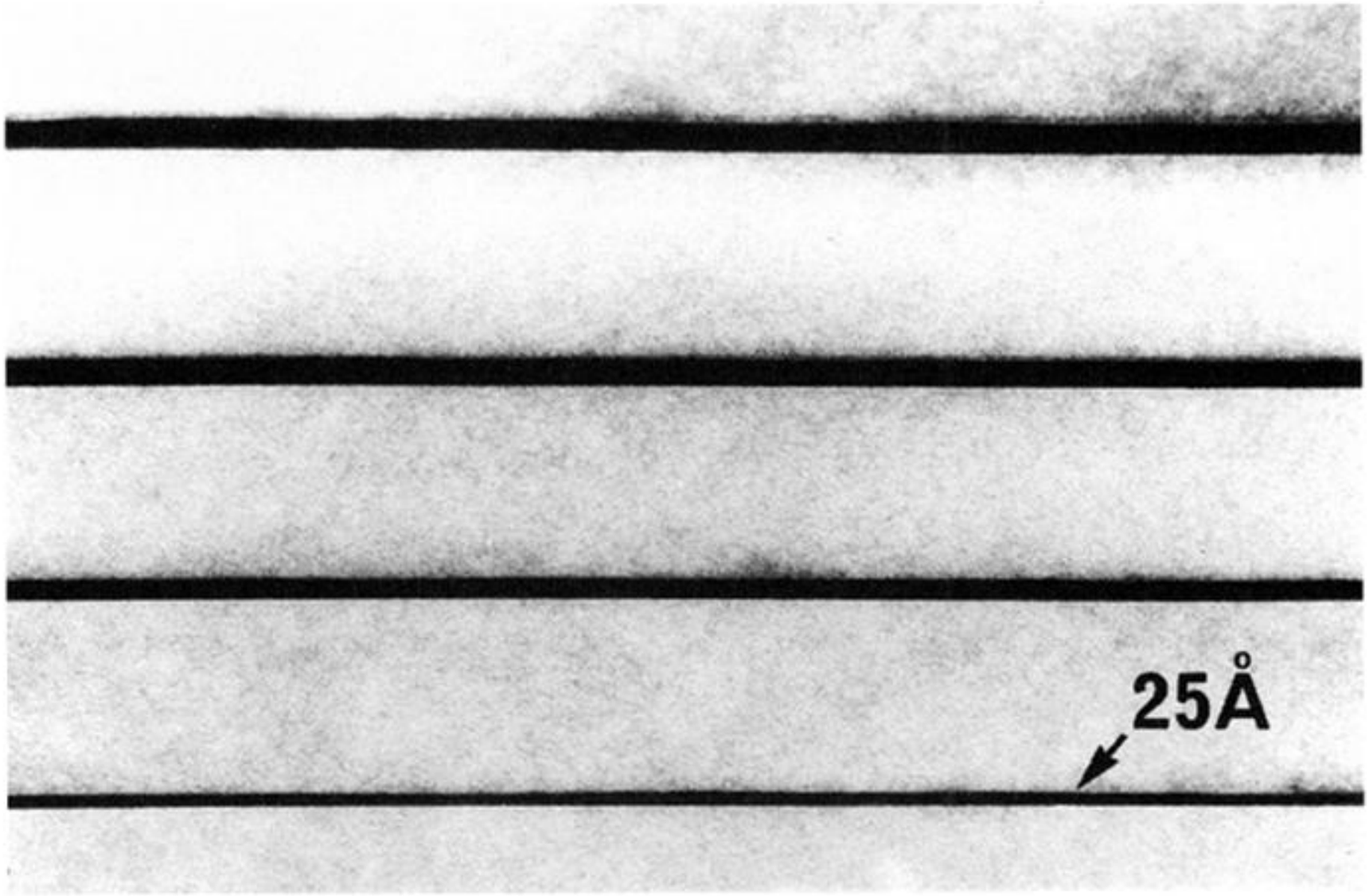


igure 1. TEM cross-sectional image, bright-field, 200 reflection, of InGaAs quantum wells (dark) in InP. (After Cullis 1990.)

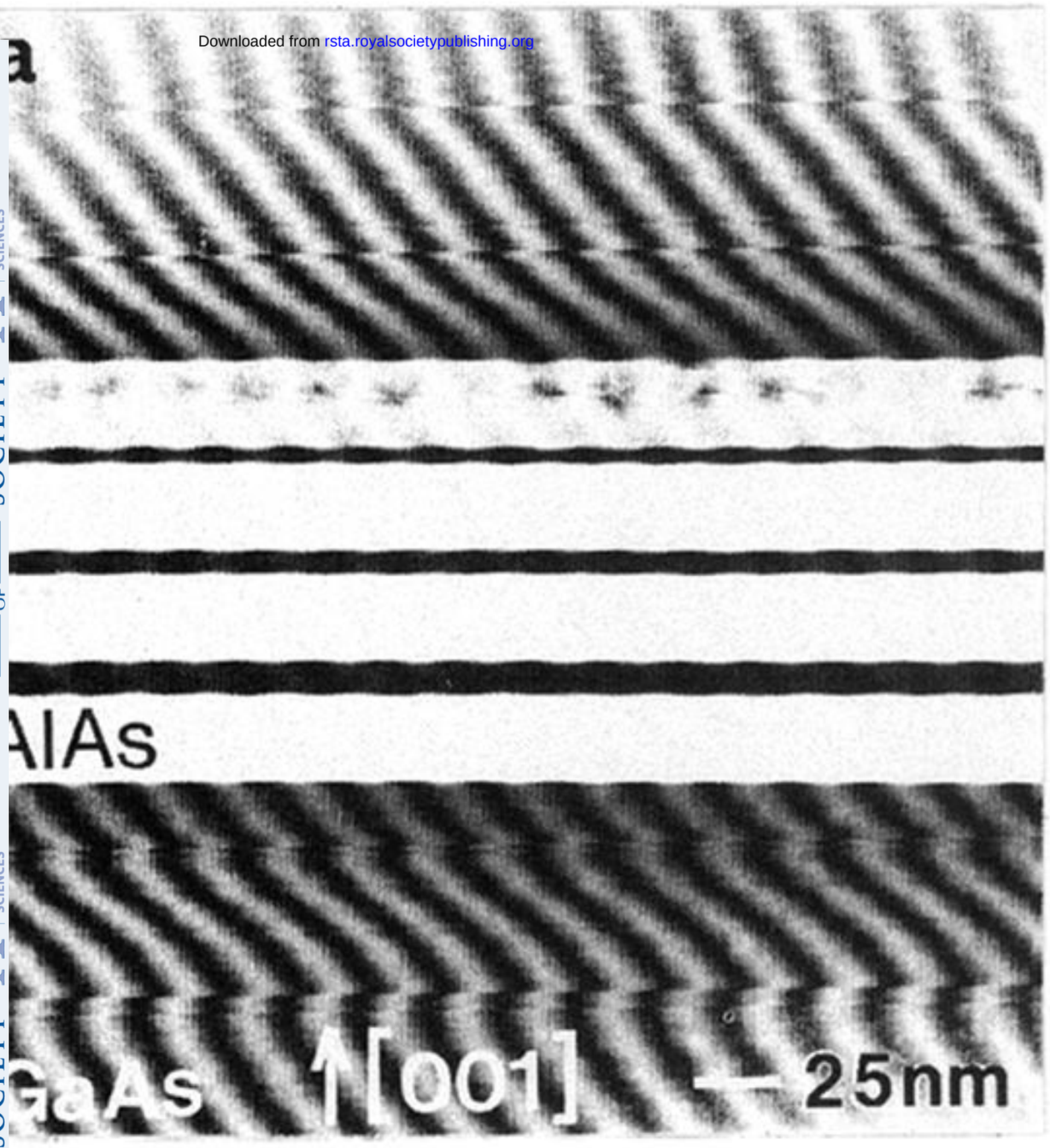
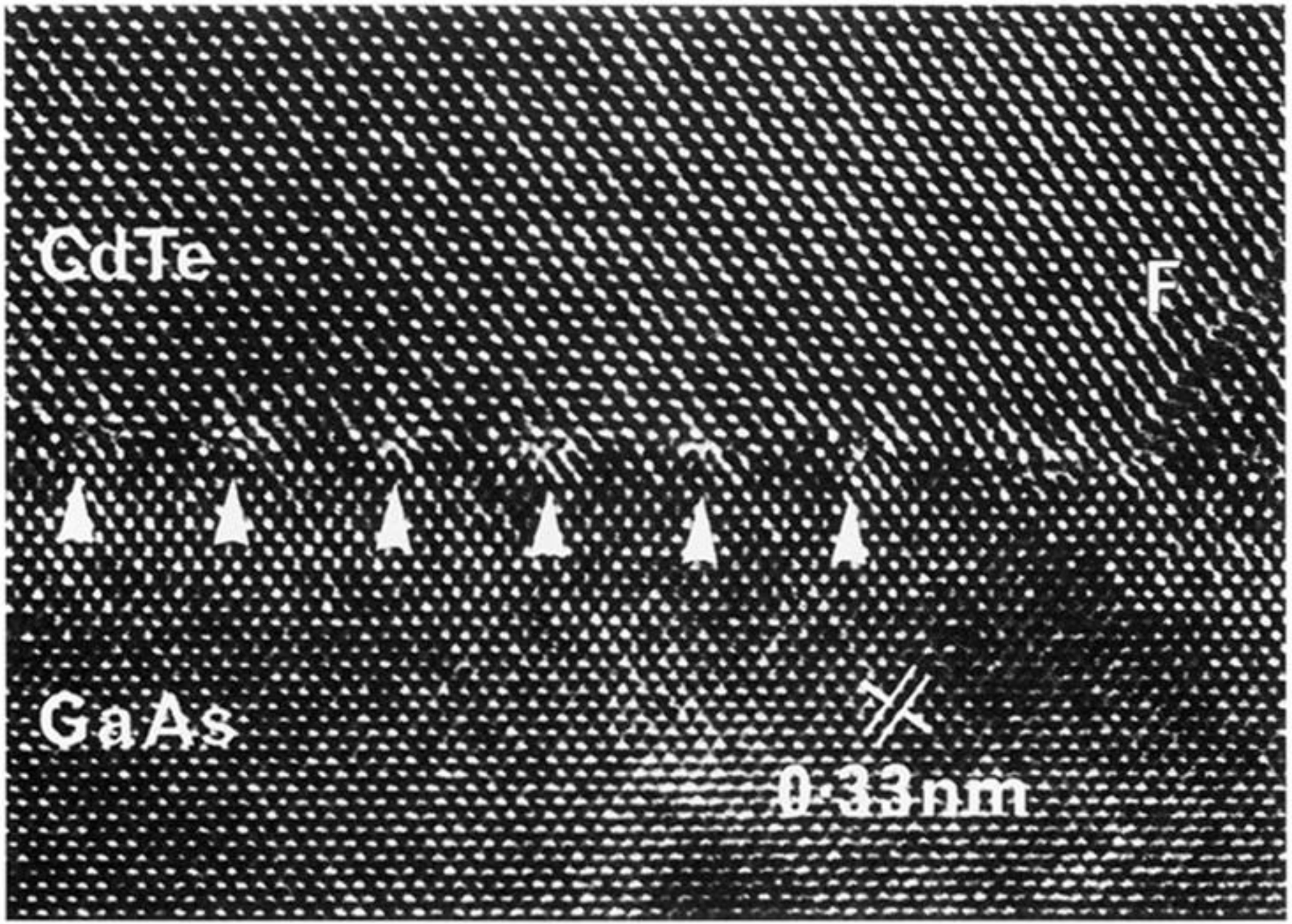
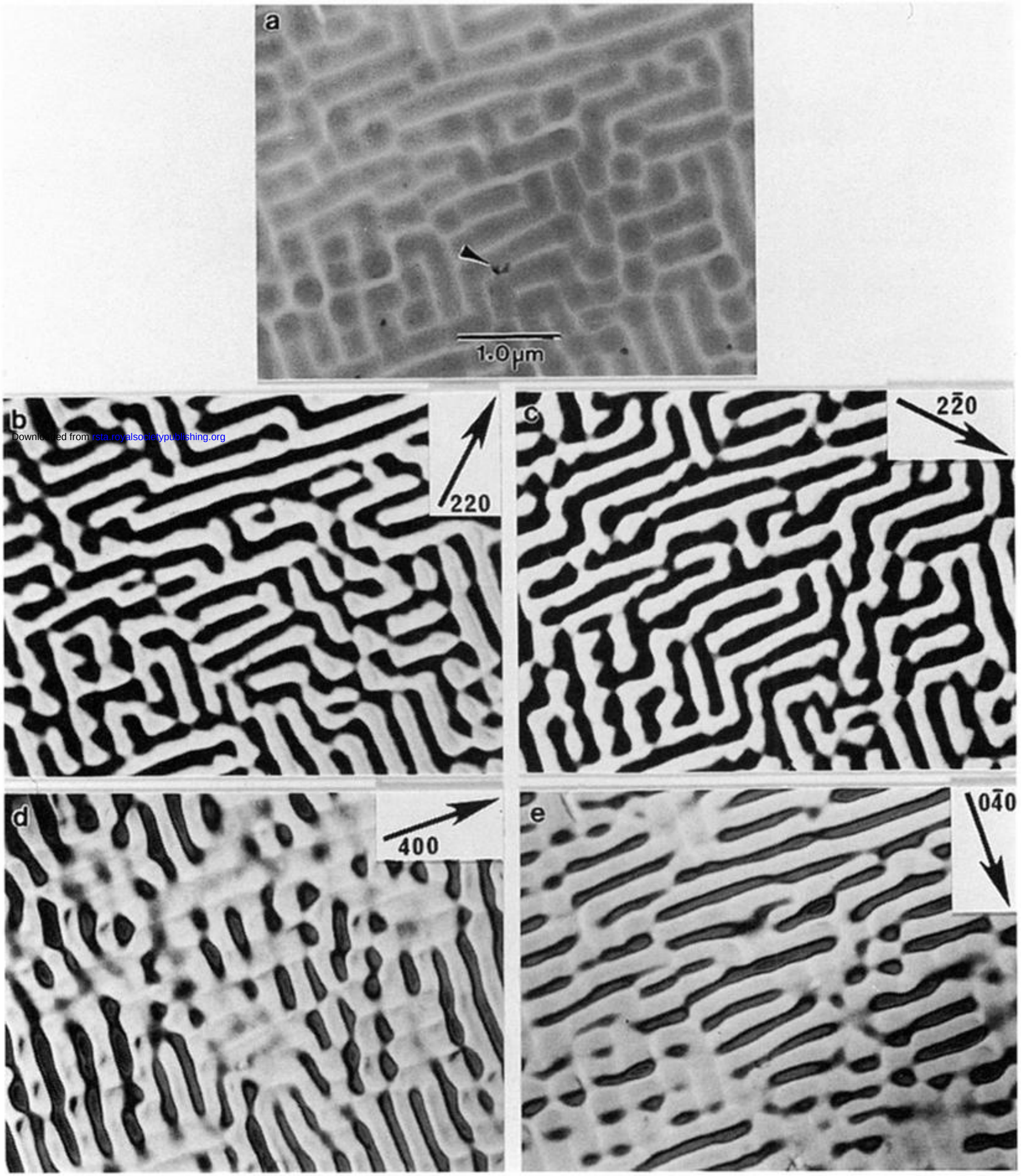


Figure 3. TEM cross-sectional images: (*a*) 200 dark-field, of GaAs quantum wells (dark) in AlAs; (*b*) processed HREM image of GaAs–AlAs quantum well showing composition variations. (After Walther & Gerthsen 1993.)

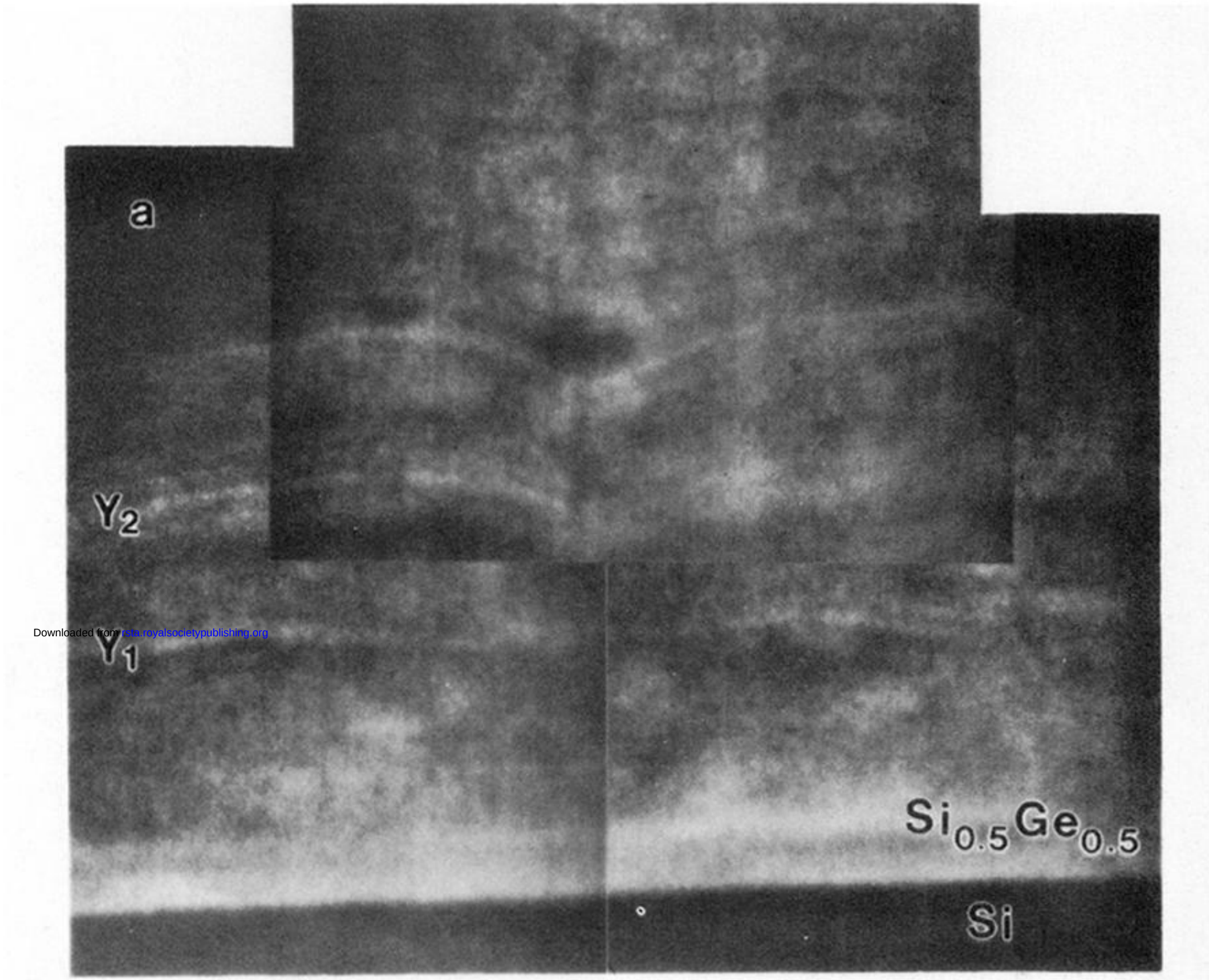


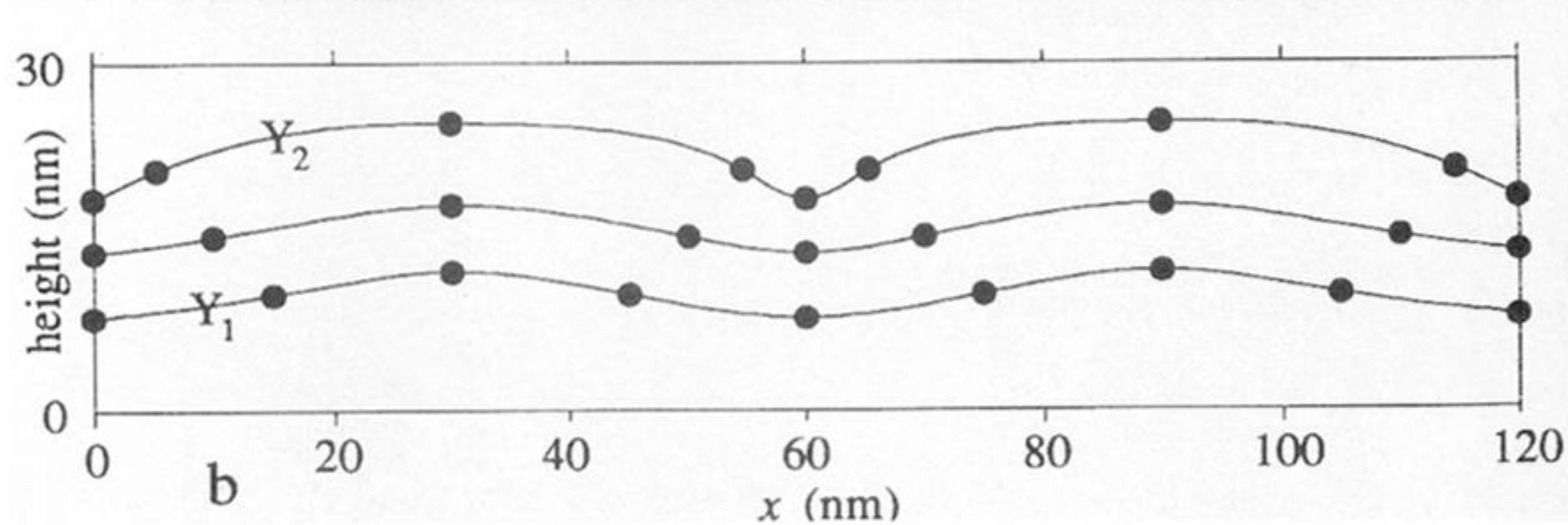
igure 4. HREM cross-sectional image along [110] direction of misfit dislocations (arrowed) at CdTe–GaAs heterointerface. Stacking fault (F) also shown. (After Cullis *et al.* 1985.)

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

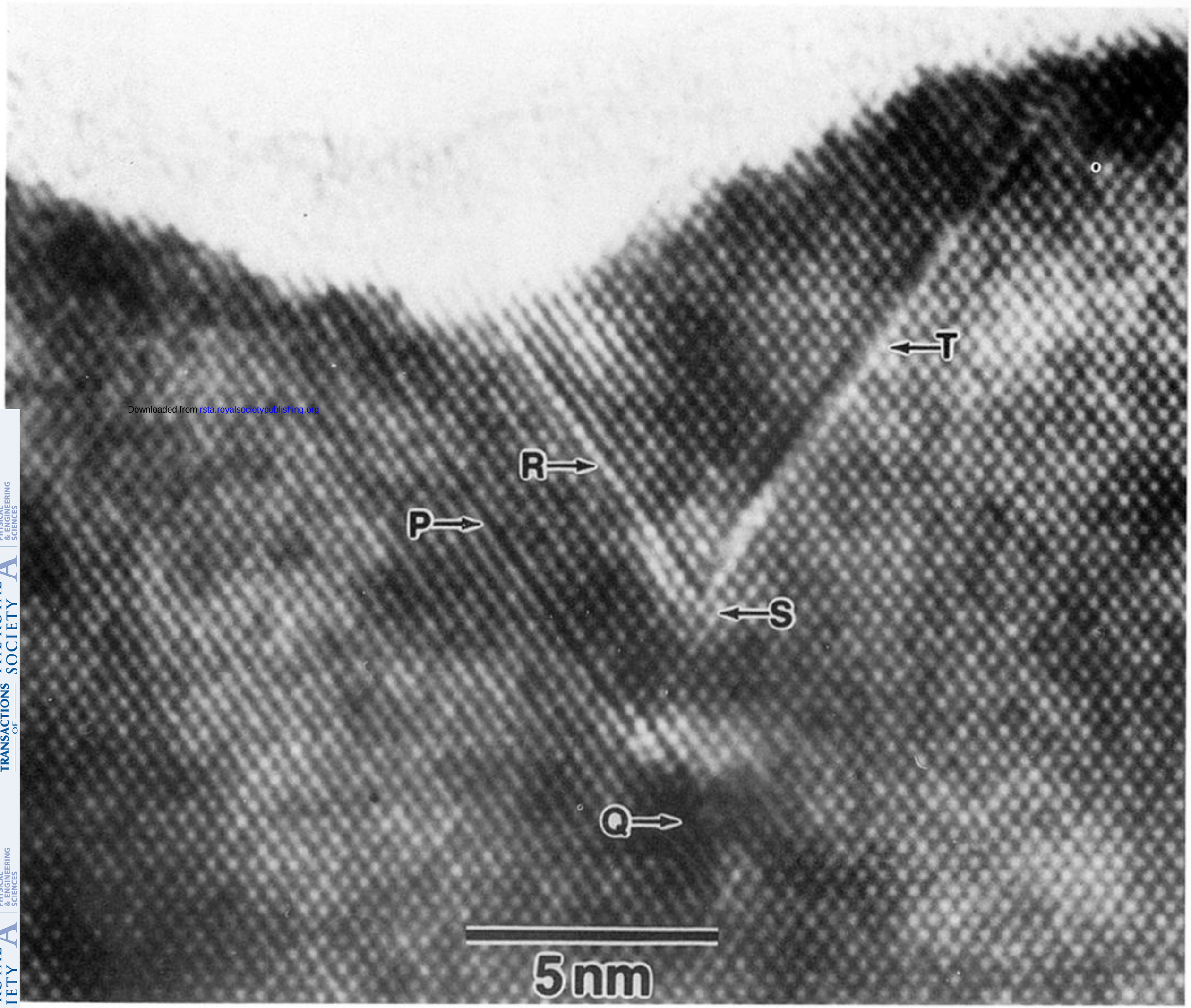


gure 5. TEM plan-view images of the same area of ripples on a growth surface of SiGe–Si. ote contrast variation with change in operating Bragg reflection. (After Cullis *et al.* 1992.)



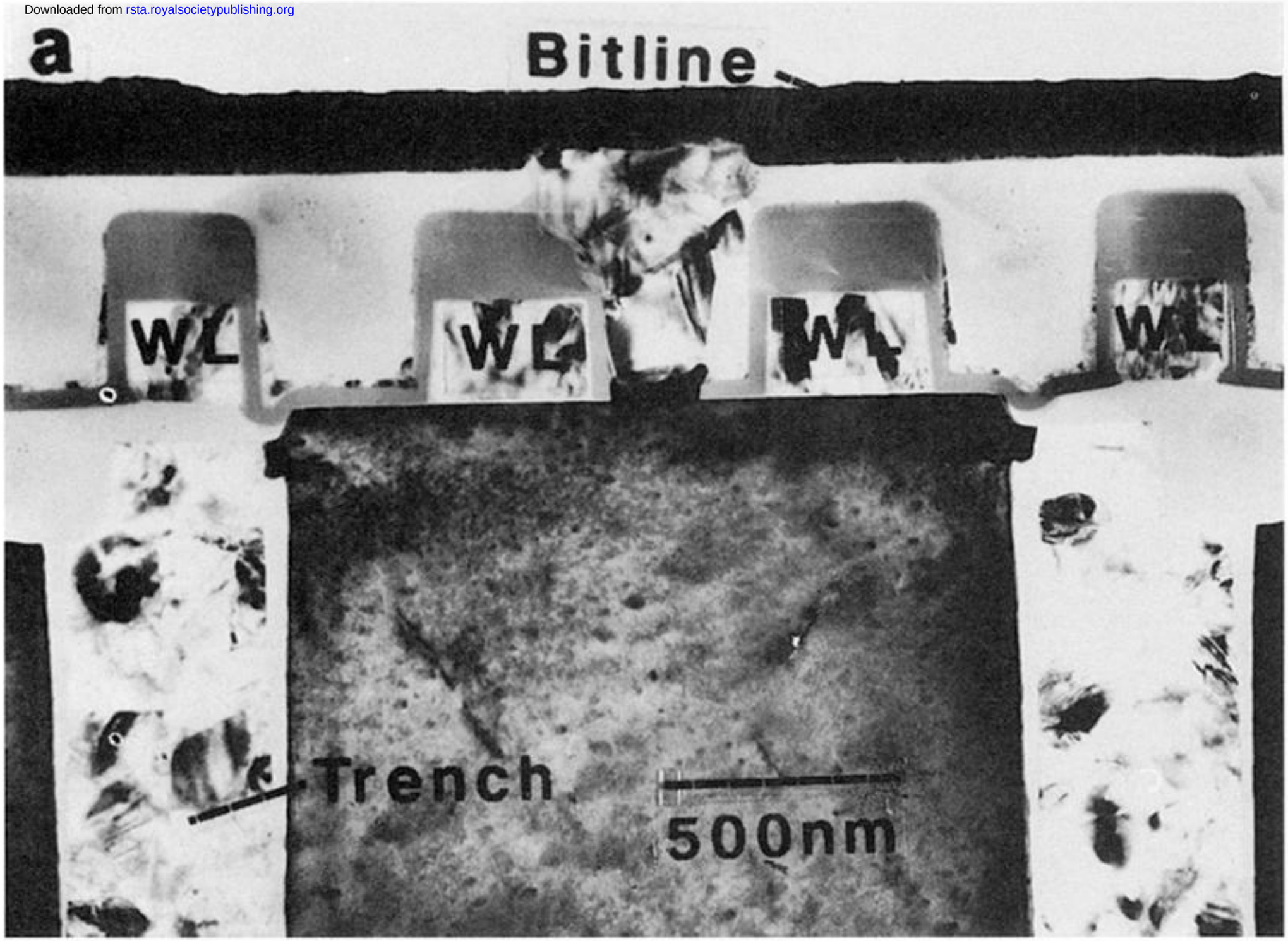


gure 6. (*a*) STEM cross-sectional image of unstable cusp formation in SiGe–Si growth surface.) Theoretical simulation of surface profile is shown in lower part of figure. (After Jesson *et al.* 93.)

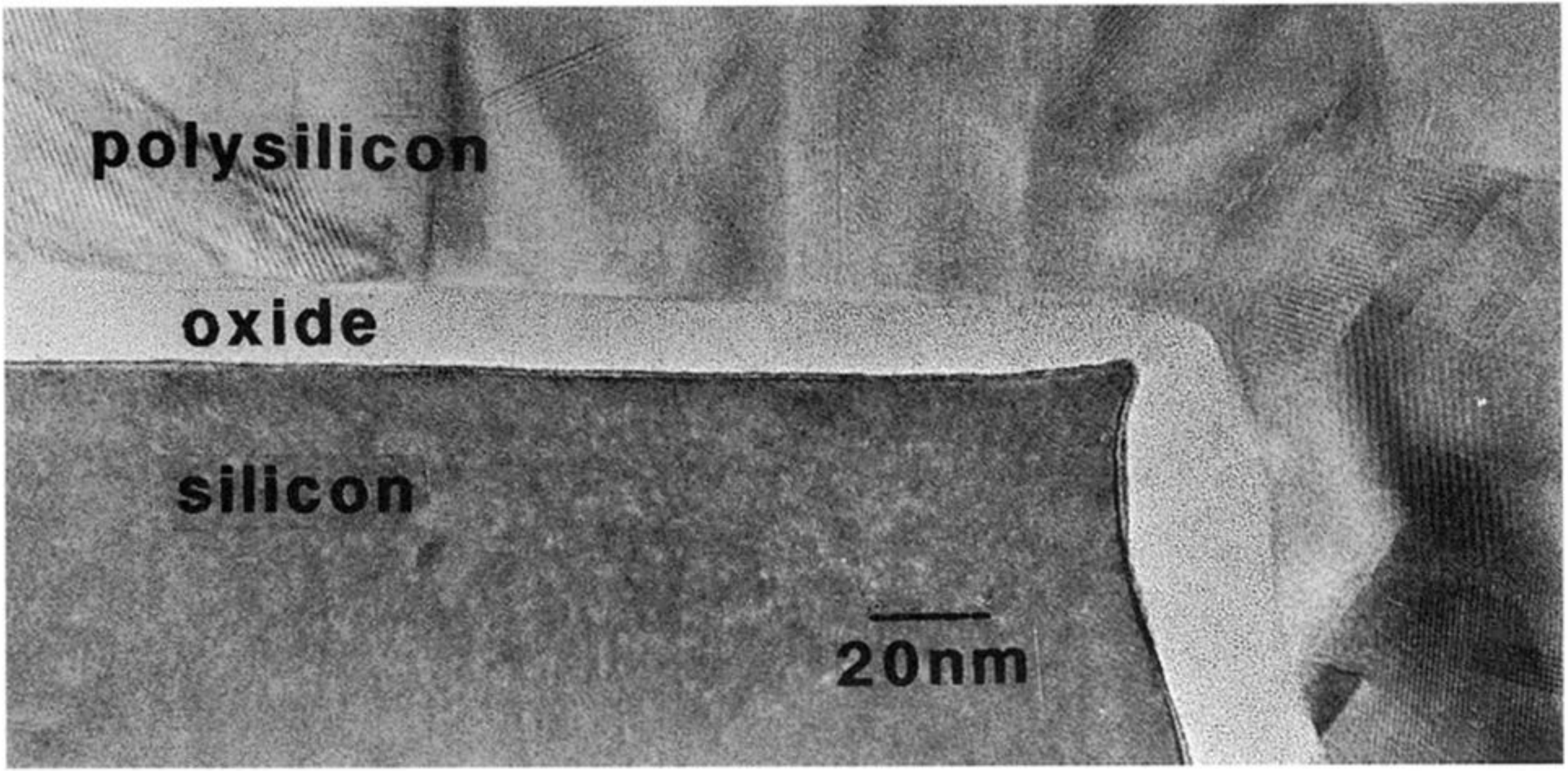


PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

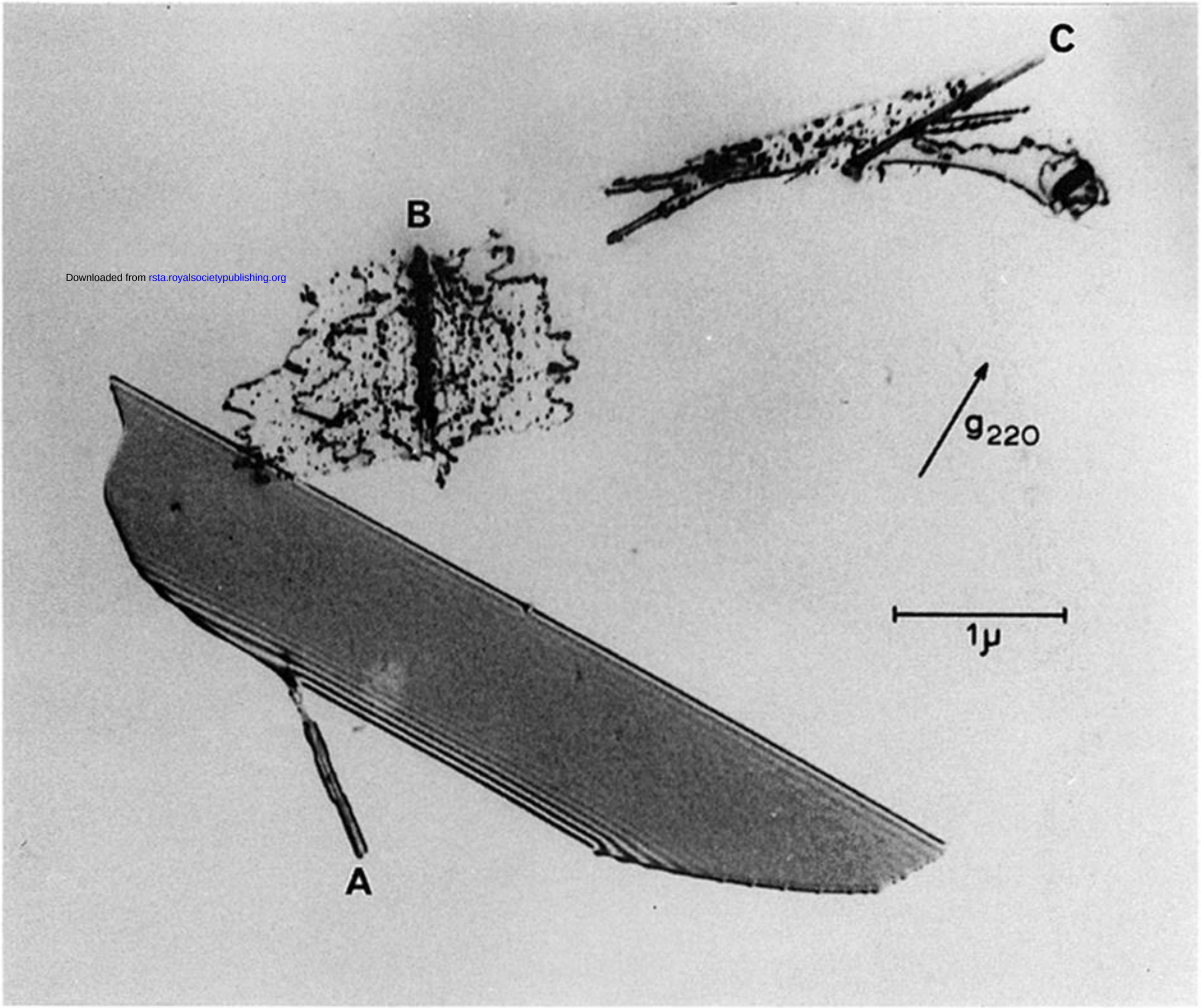
igure 7. Cross-sectional high resolution TEM image, [011] surface normal, showing misfit defects ucleated at surface ripple trough: stacking fault (P) bounded by Frank partial dislocation Q—note terminating lattice fringe parallel to fault plane) and stacking fault (R) bounded by tair-rod dislocation (S) leading to secondary fault (T). (After Cullis *et al.* 1995.)



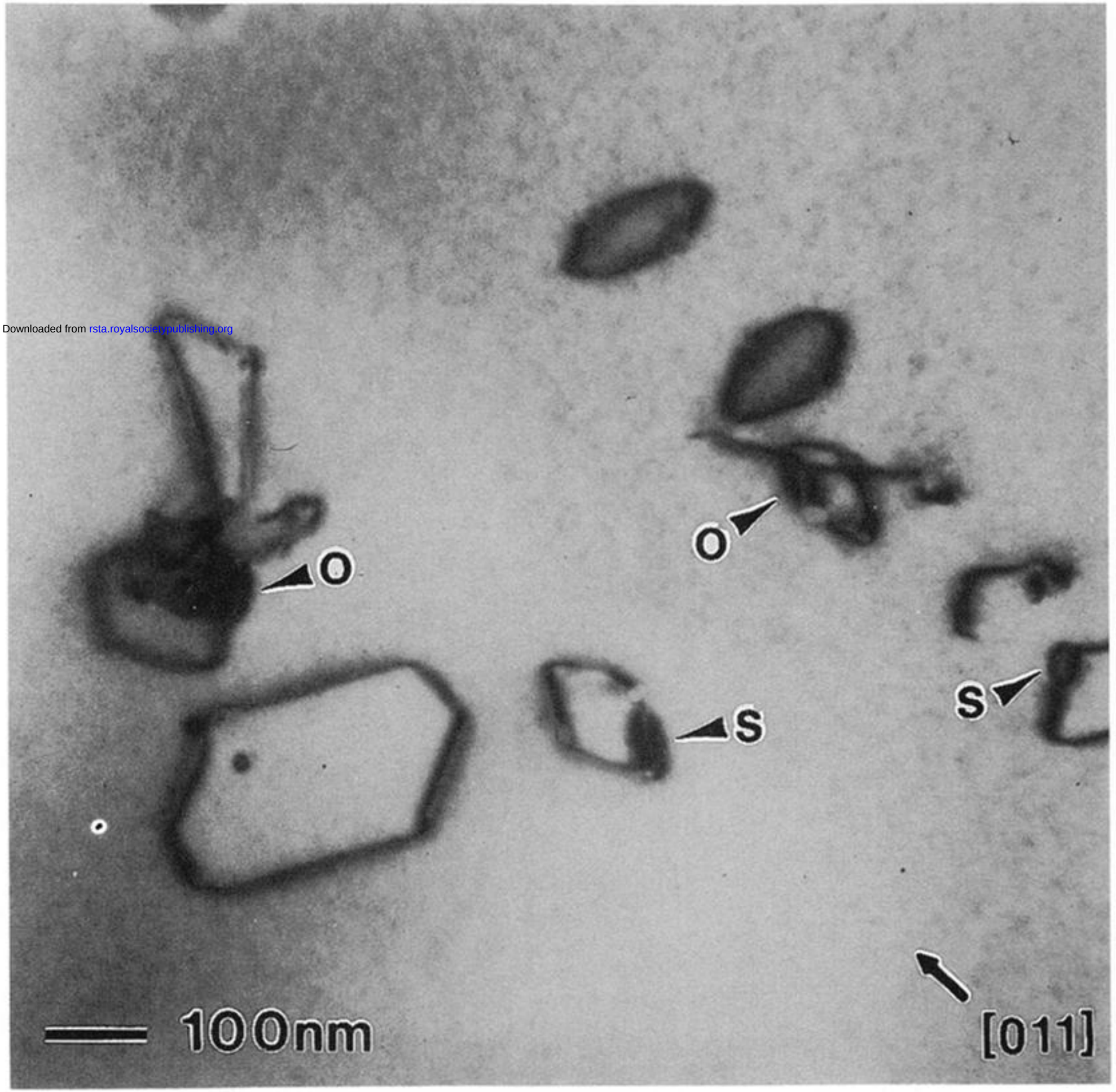
gure 8. TEM cross-sectional image of 256 Mb DRAM device structures showing layout of two cells. (After Cunningham *et al.* 1995.)



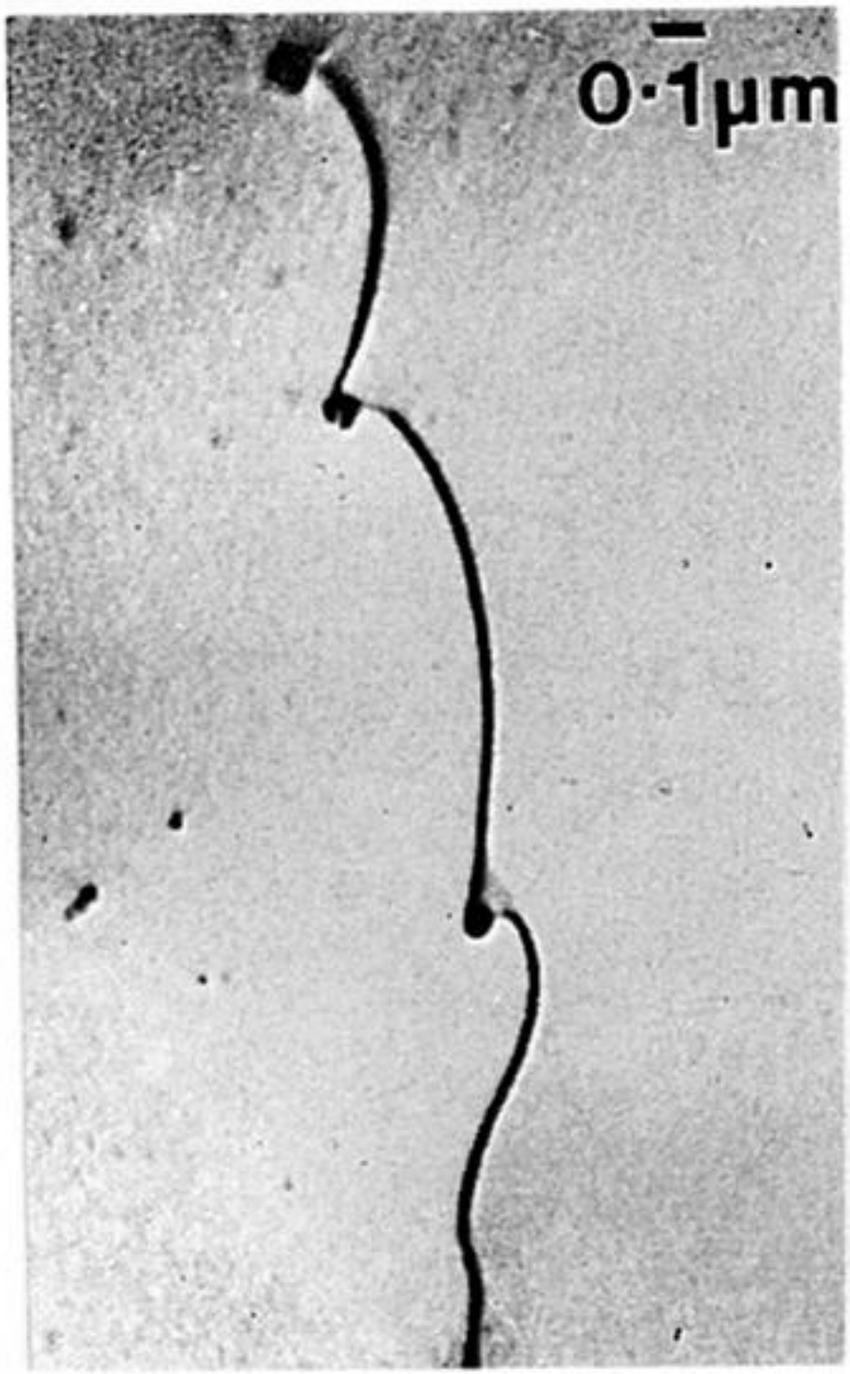
gure 9. TEM cross-sectional image of an FET thin gate oxide, showing thickness variations. (After Cunningham *et al.* 1995.)



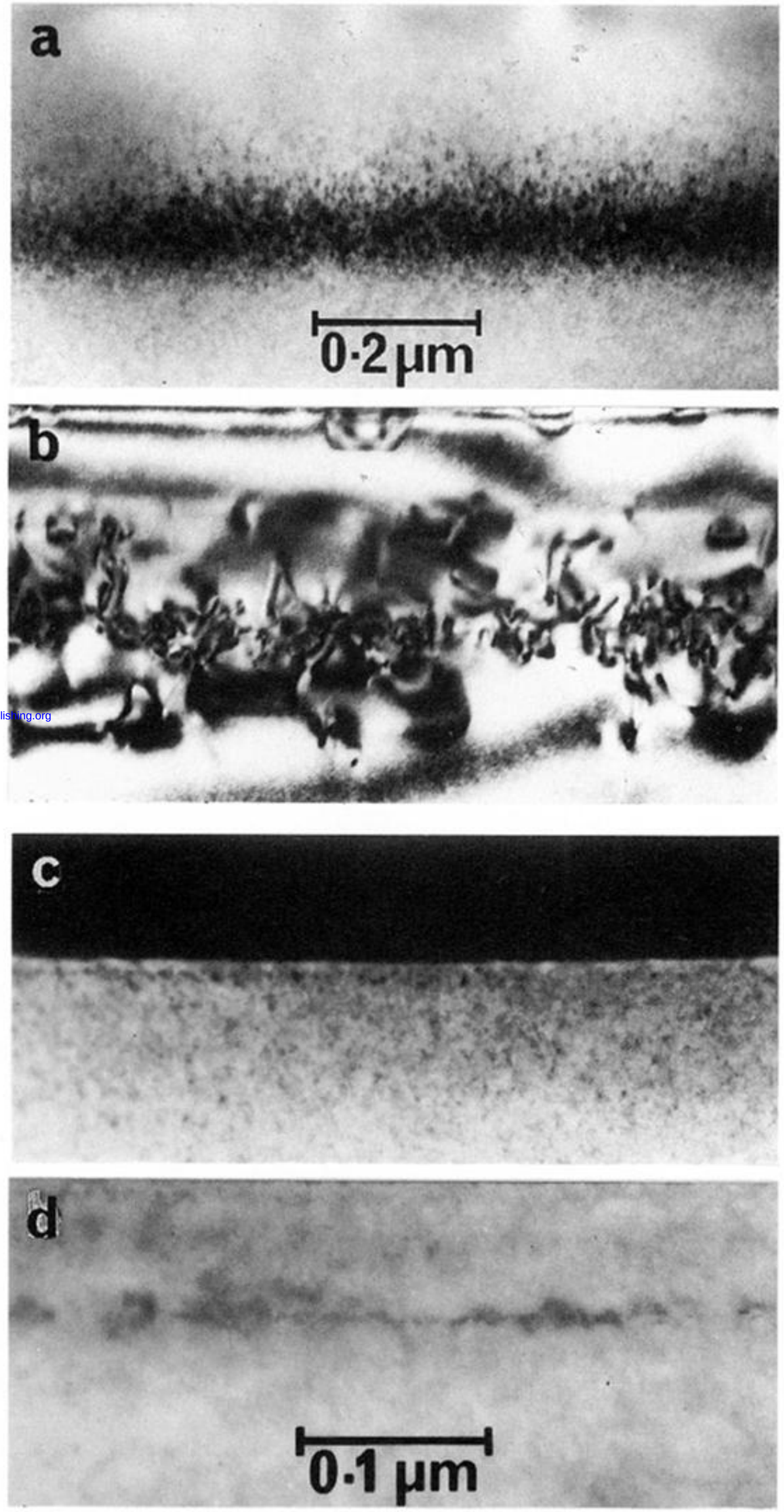
igure 10. TEM image showing inclined rod-like $FeSi_2$ precipitates A, B and C in Si, the lat-
er two also exhibiting subsidiary copper silicide precipitation. The boat-shaped feature is an
xidation-induced stacking fault. (After Cullis & Katz 1974.)



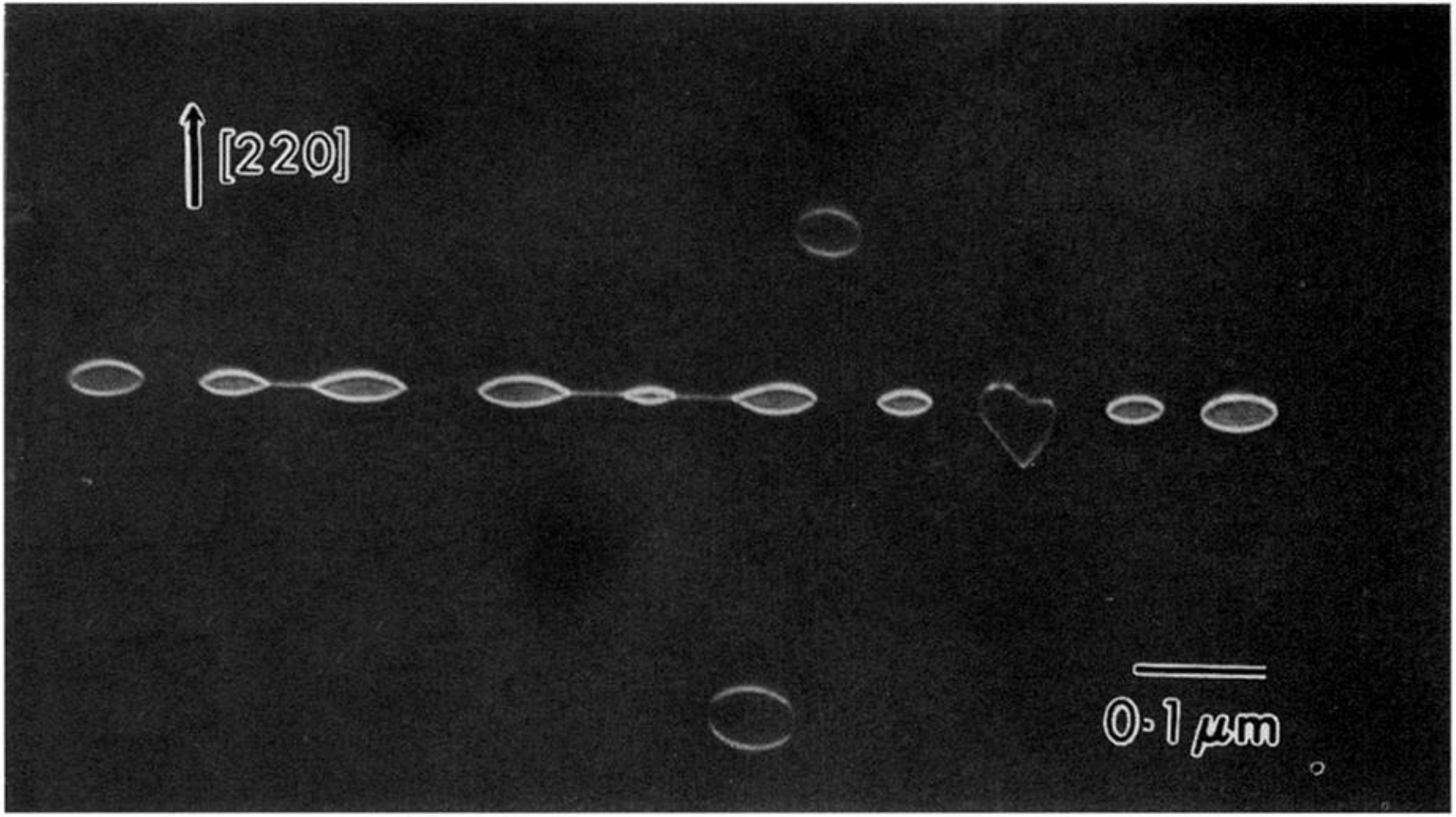
igure 11. TEM image of bulk Si, showing oxide precipitate particles (O), with array of unched-out dislocation loops which getter impurity $NiSi_2$ precipitates (S). (After Bhatti *et* . 1992.)



gure 12. TEM image of elemental As precipitates attached to dislocation in bulk GaAs. (After Cullis *et al.* 1980.)

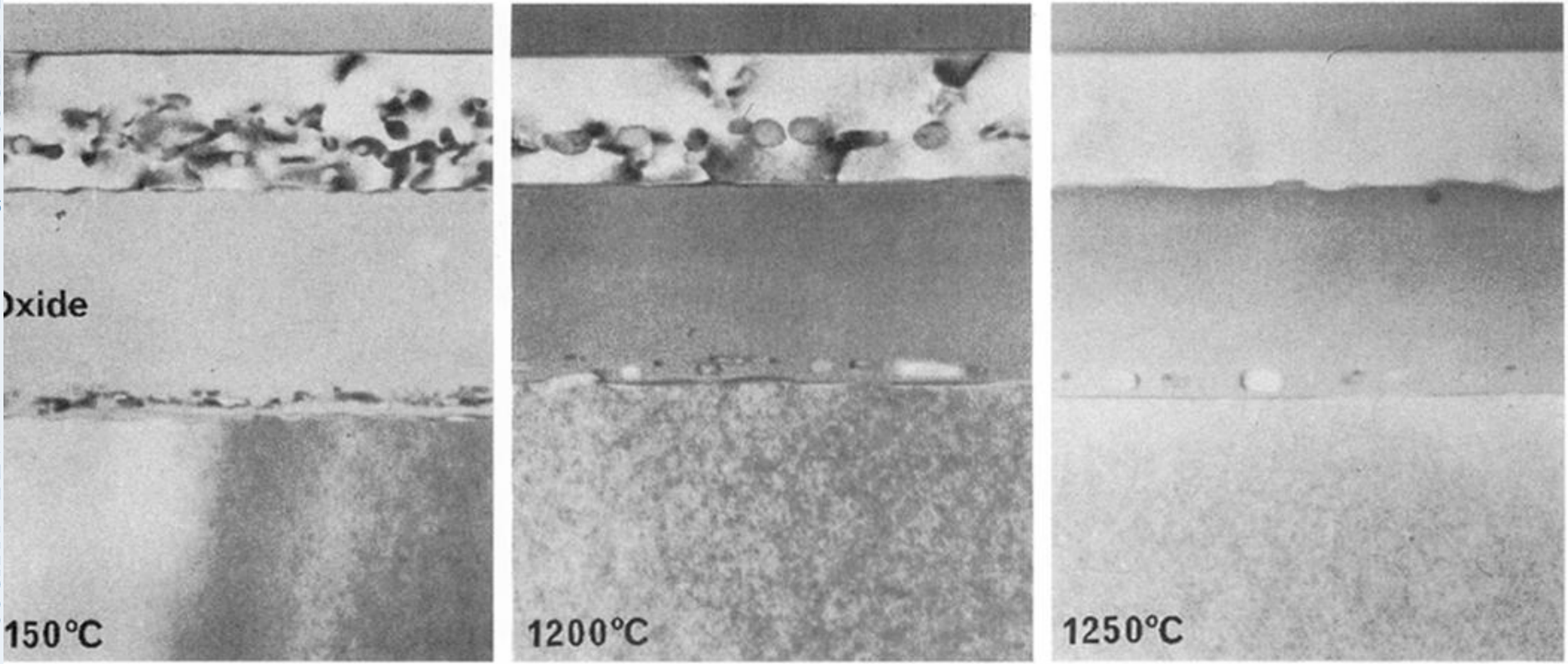


gure 13. TEM cross-sectional images of as-implanted and annealed layers, respectively, for) and (*b*) B^+ ion implantation and (*c*) and (*d*) As^+ ion implantation. (After McMahon *et al.* 80.)



igure 14. TEM image of dissociating ⟨311⟩ implantation defect giving dislocation loops. (After Eaglesham *et al.* 1995.)

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES



gure 15. TEM cross-sectional images of SIMOX layers after post-implantation anneals at the indicated temperatures. (After Augustus 1995, personal communication.)

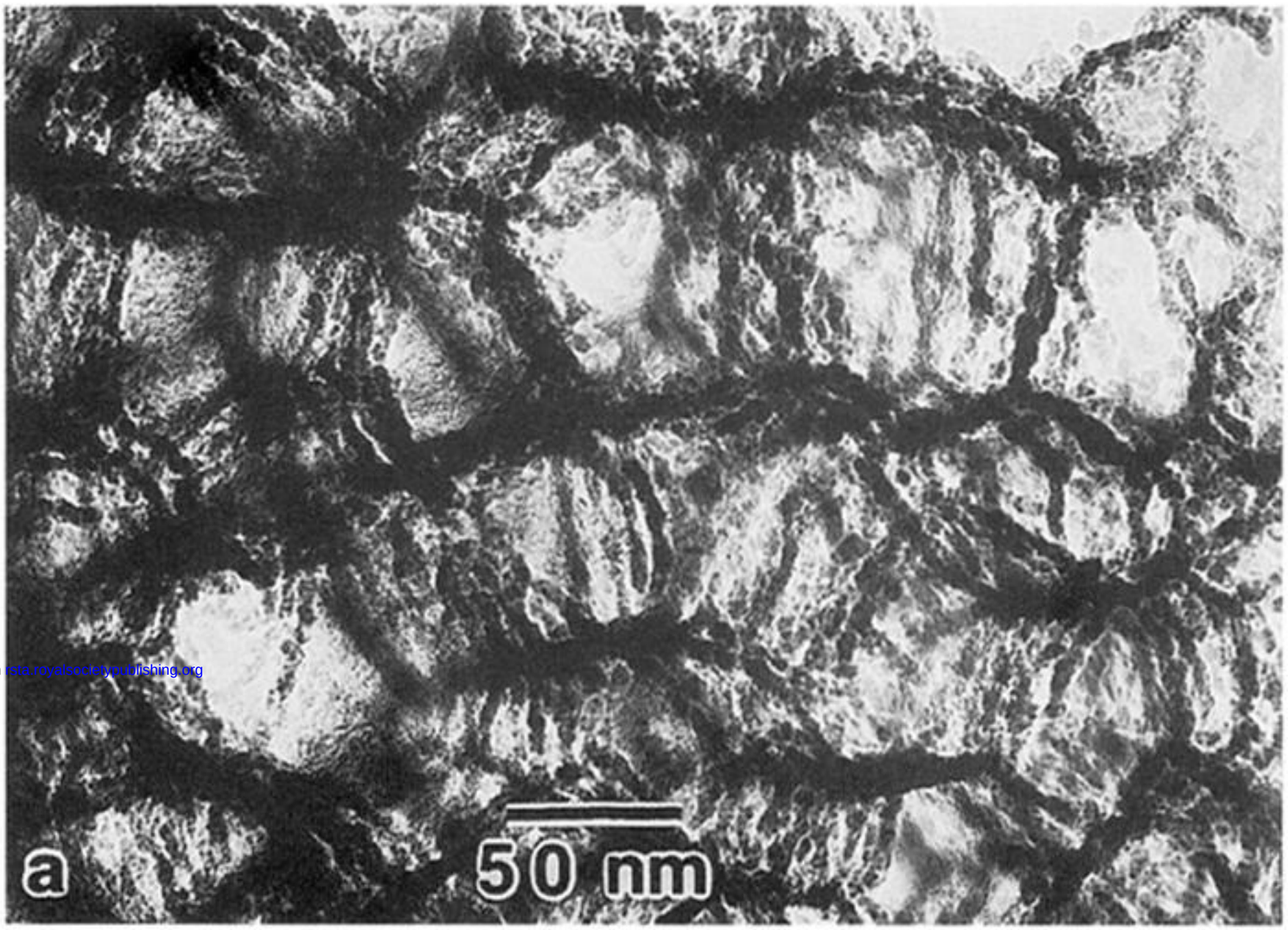


Figure 16. TEM study of nanostructures in supercritically dried porous Si: (*a*) TEM image showing undulating interconnected rods; (*b*) single crystal electron diffraction pattern showing 220 (X) and 400 (W) reflections. (After Canham *et al.* 1994.)